IEE5011 – Autumn 2013
Memory Systems
Memory Interface and GDDR5 for Graphic Applications

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Outline

- Introduction
- GDDR5 Architecture and Interface
- Data Eye Optimization
- Adaptative Interface Training
- Data Integrity and Error Detection
- Low-Power Memory
- Conclusion
- Reference
Introduction: History

- 2D 3D Graphics everywhere: Window-based operating systems, graphical user interfaces, video games, visual imaging applications, video

- GDDR2 introduced in 2003 by NVIDIA

- GDDR3 introduced in 2004 and still widely used

- GDDR5 introduced in 2008 by AMD
Introduction: Comparison with other DDR
GDDR5 Architecture

- Architecture close to DDR3 and DDR4

- 8n prefecth architecture

- Internal Buses 8x wider than I/O Buses but 8x slower
GDDR5 Architecture : OSIC Architecture
Clocking

- New: 2 different Clocks, WCK and CK
- WCK to perform reads and writes
- CK for addresses and commands
- Reducing noise and clock jitter compared to Strobe Signal from DDR3
Clamshell Mode

Standard – x32 mode

Controller

Data-Bus: 16 DQ’S

Address and Command Bus

Data-Bus: 16 DQ’S

Clamshell – x16 mode

Controller

Data-Bus: 16 DQ’S

Address and Command Bus

Data-Bus: 16 DQ’S

GDDR5 – (x16 mode)
Memory Controller-Core Interface

Controller

- Number of pins: 61 pins
- 2 pins for EDC0+EDC1
- 2 pins for WCK
- 36 pins for Byte 0,1: DQ's + DBI and Byte 2,3: DQ's + DBI
- 2 pins for WCK
- 2 pins for EDC2+EDC3
- 9 pins for Address Bus + ABI
- 5 pins for Command Bus
- 2 pins for CK
- 1 pin for Reset

GDDR5 - DRAM

- Data Bus
- Address and Command Bus
Data Bus Inversion

<table>
<thead>
<tr>
<th>Signals</th>
<th>Transmitted Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ0</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>DQ1</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>DQ2</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>DQ3</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>DQ4</td>
<td>1 0 1 1</td>
</tr>
<tr>
<td>DQ5</td>
<td>1 1 1 1</td>
</tr>
<tr>
<td>DQ6</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>DQ7</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>/DBI0</td>
<td></td>
</tr>
</tbody>
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<tr>
<th>Data Bus</th>
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<tbody>
<tr>
<td>1 0 1 1</td>
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<tr>
<td>1 1 1 1</td>
</tr>
<tr>
<td>1 1 0 0</td>
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<td>1 1 1 0</td>
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<td>0 0 0 1</td>
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</tbody>
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<table>
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<tr>
<th>Received Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 1</td>
</tr>
<tr>
<td>0 1 0 1</td>
</tr>
<tr>
<td>0 1 1 0</td>
</tr>
<tr>
<td>0 1 0 0</td>
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<td>1 0 1 1</td>
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Data Eye Optimization

- I/O interface signals need good quality for high data rate

- Problems of crosstalk noise and inter-symbol interference cause jitter in the interface between controller and memory core
Data Latching
Auto-Calibration Engine
Unmatched Trace Length Routing
Adaptative Interface Training

- Problem with high data rates: lower timing margins
- Voltage and temperatures changes + impedance mismatch

- Solution = Training, which provides stability
- Done by memory controller
- Align all the signals
- CK = reference signal
Adaptative Interface Training Sequence

GDDR5 training sequence
- power-up
- address training
- CK2WCK phase adjust
- READ training
- WRITE training
- EXIT
Clock Training

![Diagram]

- WCK
- CK
- \( \div 2 \)
- EDC
Read Data Training
Result of Adaptative Training
Error Detection using CRC Algorithm
Parallel Calculation of DBI and CRC
Lower the Power Consumption

- Using DVFS
- Technology Shrinking
- Data Bus Inversion
- Auto-Engin Calibration

Switching between Different Modes:
  - Full Mode
  - Power-down mode
  - Self Refresh Mode
Power Saving by Voltage Reduction

- 68 nm 1 G GDDR3 (1.8V) 256 bits: 11 W
- 56 nm 1 G GDDR3 (1.8V) 256 bits: 7.3 W (34% Savings)
- 46 nm 2 G GDDR3 (1.8V) 256 bits: 5.9 W (19% Savings)
- 46 nm 2 G GDDR5 (1.5V) 128 bit: 4.3 W (27% Savings)

Total Savings: 61%
Conclusion

- GDDR5 = Low Power + High Data Rate Memory
- GDDR5 is still improved
- GDDR5M in 2014 for Small Devices
- Increasing Data Rate = Problem: Heat dissipation and consume too much energy
- Solution = GDDR6?
- GDDR6 announced for 2014 but JEDEC specification is late.
References

- Qimonda GDDR5 - White Paper, August 2007
- Jinyeong Moon and Joong Sik Kih, Fast Parallel CRC & DBI Calculation for High-speed Memories: GDDR5 and DDR4, May 2011