A 16kB Tile-able SRAM Macro of an Operating Window of 4.8GHz at 1.12V VDD to 10MHz at 0.5V in a 28-nm HKMG CMOS

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Outline

• Motivation
• 16kB SRAM Macro
  – Implementation
  – Circuit Optimization for Low Voltage
• Independently Controlled Precharge and Write Driver (ICPW)
• Measurement Results
• Conclusion
Motivation

• The increasing demand for high performance and low power devices in mobile applications

• Dynamic voltage and frequency scaling (DVFS) technique has been applied widely.

• Develop a tile-able embedded SRAM IP with a wide operating voltage range to meet DVFS.
  – L1 cache application
Published High Performance SRAMs

- Compared to 32nm designs @ 4GHz
  - 4% smaller VDD
  - Roughly 10~12% power reduction
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- 16kB array takes **Cycle 2 and 3**
- Tiled for more than 16kB: Two extra cycles (**Cycle 1 and 4**)

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**Floor Plan & Pipeline Diagram**

- **Cycle 1**: Pre-decode Distribution
- **Cycle 2**: 16kB Array Decode
- **Cycle 3**: 16kB Array Access
- **Cycle 4**: Output Distribution

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- **4kB** and **4kB**
- **Write Driver** and **Ctrl**
- **Read Out Latch**
- **MUX Latch**
Critical Path of 16kB SRAM Macro

- 16 cells/BL
- Single-ended sensing scheme
- Dynamic-to-static read latch
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Cross-Coupled PMOS Analysis

- **Cross-Coupled PMOS keeper**
  - Better noise immunity but slower read out speed
- **NAND2 with higher PN ratio**
  - Faster read out speed but worse noise immunity
• VBL discharges faster at low VDD and high T due to increasing leakage.
  – It may cause read “1” fail.
Read “0” Delay Comparison

- **Read-0 delay without keeper**
- **Read-0 delay with keeper**

Keeper with high PN ratio $ND2 \approx$ Without keeper

![Graph showing read “0” delay comparison](image)

- Vertical axis: WL to ND2 Output Delay (ps)
- Horizontal axis: PN Ratio of ND2

Key points:
- The graph illustrates the delay comparison between with and without a keeper for different PN ratios of ND2.
- The dashed line represents the delay with a keeper, while the solid line represents the delay without a keeper.
- The arrow indicates the direction of increasing PN ratio and the corresponding increase in delay for both cases.
- The keeper with a high PN ratio results in a delay that is approximately equal to the delay without a keeper for the given PN ratio range.

This graph is crucial for understanding the impact of keepers on the delay characteristics of memory elements in digital systems.
Keeper size is a tradeoff between read “0” speed and glitch.
Minimum GBL Voltage vs. Keeper Size

- At lower VDD, GBL voltage degrades faster.
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The magnitude of drop depends on the bitline loading.
If the Cross-Coupled PMOS is turned on, it makes write time longer.
A potential short current between precharge PMOS and write driver NMOS.
Precharge is simultaneously terminated with a write. ➞ No short current
Bit Line Behavior

- Bitline could be driven before WL activation.
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Die Photo and Characteristic Summary of 16kB SRAM

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 28nm HKMG bulk CMOS</td>
</tr>
<tr>
<td>Cell</td>
<td>0.156um² high current 6T SRAM</td>
</tr>
<tr>
<td>Bit Line Scheme</td>
<td>16 cells/BL single-ended sensing(NAND2)</td>
</tr>
<tr>
<td>Organization</td>
<td>512 row x 2 column x128</td>
</tr>
<tr>
<td>16kB Macro Area</td>
<td>0.051mm²(0.207mm x 0.243mm)</td>
</tr>
<tr>
<td>Redundancy</td>
<td>Column shift type</td>
</tr>
</tbody>
</table>
High Frequency Shmoo

4 Monitor Pads In UHFT Test Chip

- 4.8GHz @ 1.12V
- 4GHz @ 0.96V
- 1.92GHz @ 0.72V
Low VDD Shmoo
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Conclusion

- A 16kB tile-able 6T SRAM IP has an operating window of 4.8GHz at 1.12V to 10MHz at 0.5V in TSMC 28nm HKMG process.

- Circuit considerations and improvements for DVFS.
  - Cross-coupled PMOS keeper and NAND2 with higher PN ratio to achieve faster read speed and better noise immunity
  - Keeper size optimization for low voltage
  - ICPW for faster write speed