µ-SPI: A Low Power On-Interposer Bus for 2.5D Heterogeneously Integrated Biomedical Microsystems

Po-Tsang Huang[1], Yu-Rou Lin[1], Kuan-Neng Chen[1], Jin-Chern Chiou[1], Ching-Te Chuang[1], Wei Hwang[1], Kuo-Hua Chen[2], Chi-Tsung Chiu[2], Sog Yang[2] and Ho-Ming Tong[2]

[1] National Chiao Tung University, [2]Advanced Semiconductor Engineering (ASE) Group, Taiwan

ABSTRACT

In this paper, an on-interposer bus (µ-SPI, serial peripheral interface) is proposed for providing low power data communication in 2.5D heterogeneous integrations. The protocol of µ-SPI is designed based on the physical layer of SPI. To reduce the overhead of the header, the header of a packet is divided into two levels by the hierarchical packetization technique. Moreover, a pseudo multi-master is proposed to replace the arbitration circuits via master passing. The proposed µ-SPI is utilized in a 2.5D heterogeneously integrated bio-sensing microsystem, and the average power of this on-interposer bus is only 23.2 µW at 1.8V and 100 KHz.

1. INTRODUCTION

System-in-package (SiP) can provide enormous advantages in achieving heterogeneous integration, microminiaturizing form factor, improving system speed and reducing power consumption for future generations of ICs. Among different SiP technologies, through-silicon-via (TSV) 3D integrations have emerged as a solution in developing SiP integration [1]. However, stacking multiple dies would face severe challenges of the increasing cost and thermal effect due to the low thermal conductivity of inter-layer dielectrics and high power density [2]. Therefore, TSV 2.5D integrations have been proposed as an evolved solution for reducing the overall cost and avoiding thermal effects from 3D-ICs [3, 4]. Different from TSV 3D integrations, the tiers of a 2.5D design are bonding on the top of a silicon interposer.

Silicon interposer consists of low-k material interconnections and Cu TSVs in a silicon substrate and performs as a reliable connection between chip and organic substrate cooperating with micro-bumps and TSVs. An interposer provides inter-chip communication between multiple chips via redistribution layers (RDLs) enabling bandwidth improvement, power reduction and very good heat spreading [4]. In this paper, an on-interposer bus, µ-SPI (Serial Peripheral Interface), is proposed for providing low power data communication in 2.5D heterogeneous integrations.

2. µ-SPI: LOW POWER ON-INTERPOSER BUS FOR TSV 2.5D INTEGRATION

On-interposer buses are developed for providing energy-efficient data communication in TSV 2.5D integration. Additionally, on-interposer bus protocols are designed to transfer data between different dies mounted on the interposer. Table I presents the comparisons between on-interposer buses, PCB buses and on-chip buses. Both on-interposer buses and PCB buses are developed for inter-chip communication, and on-chip buses is utilized for intra-chip communication between IPs.

Table I. Comparisons between PCB, on-chip and on-interposer buses.

Bus Type	Pin Number	Speed	Power
PCB Bus (A)	Few	Slow	Large
On-Interposer Bus (B)	Medium	Fast	Small
On-Chip Bus (C)	Many	Very Fast	Very Small
Comparisons	A < B << C	C > B >> A	A >> B >> C

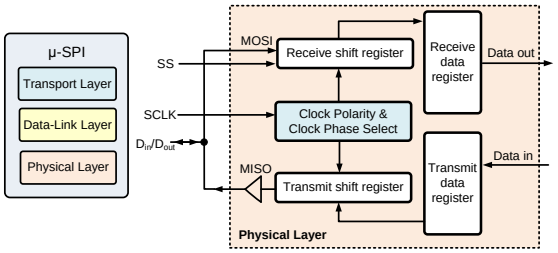

Fig. 1. Three abstract layers of µ-SPI.

2.1. Abstraction Layers of µ-SPI

Based on the characteristics of on-interposer buses, the protocol of the proposed is designed using three abstraction layers as shown in Fig. 1. The transport layer provides end-to-end communication services for the overall systems. Additionally, the transport layer provides convenient services such as connection-oriented data stream, reliability, flow control, and low power bus coding. In the transport layer of µ-SPI, the back-end interface can adopt cyclic redundancy check (CRC) and crosstalk avoidance coding (CAC) for providing low-power and reliable data communication.

In the data-link layer of µ-SPI, the master controls the data bus by generating the clock signal (SCLK) and corresponding headers for all slaves. The µ-SPI can provide point-to-point or broadcast communication, half duplex or full duplex transmission and received-controlled acknowledgment. Hence, the header contains the addresses of the selected slaves and creates the links between the corresponding devices. Moreover, the µ-SPI can support pseudo multi-master via mater passing technique.

The physical layer is implemented to synchronize signals according to the standard SPI [5] but with bidirectional links as shown in Fig. 1. The signal SS (Slave Selection in SPI) is used to indicate the valid period of each packet. Additionally, the data width of µ-SPI can be extended from 1-bit to 8-bit.

2.2. Hierarchical Packetization

To reduce the overhead of the header, the header of a packet is divided into two levels by the hierarchical packetization technique as shown in Fig. 2. The length of 1st level header is fixed as 12-bit for indicating the functionality of this packet. Based on the information of 1st level header, the 2nd level

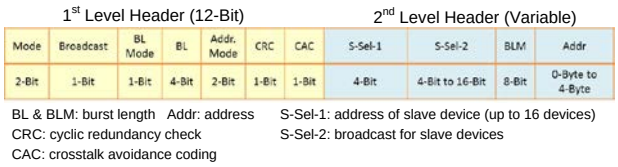

Fig. 2. Hierarchical header.

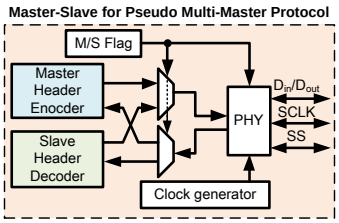

Fig. 3. Master/slave device for pseudo multi-master.

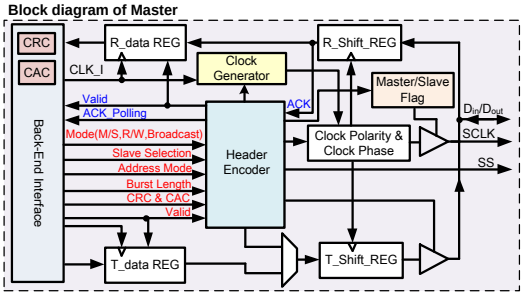

Fig. 4. Block diagram of master module.

header is variable for providing wide range of the burst length, broadcasting or point-to-point selection and variable length of addresses.

2.3. Abstraction Layers of μ-SPI

The pseudo multi-master is proposed in μ-SPI to replace the complex arbitration circuits via master passing. All the master devices are implemented as master/slave modules as shown in Fig. 3. Therefore, a master/slave device can be either a master or a slave, and only 1 master can exist in the master/slave modules by controlling MS_Flag. The M/S flag indicates the direction of SS, SCLK and data. If the M/S flag is one in a Master/Slave device, this device is the only master in μ-SPI until passing this flag to the other master/slave device via a specific packet. In view of this, the 1st level header contains a pseudo multi-master mode for master passing.

2.4. Design of Master Module & Slave Module

The block diagram of a master module and a slave module are as shown in Fig. 4 and Fig. 5, respectively. In the master module, the back-end interface transfers the communication mode, selected slaves, address mode, burst length and valid bit to the header encoder for generating hierarchical packets. The slave is constructed by the two-layer header decoder and PHY, the white blocks in Fig. 5. The slave receives SS & SCLK signals from the master to decode packets. The SS signal is used to indicate the valid period of each packet and controlled by the master.

3. μ-SPI IMPLEMENTATION FOR A 2.5D HETEROGENEOUS MICROSYSTEM

A heterogeneously integrated neural-sensing microsystem is implemented on an interposer with 4 dies fabricated by 65nm and 180nm CMOS technologies as shown in Fig. 5. The proposed μ-SPI is implemented in this 2.5D microsystem to provide the on-interposer communication between these 4 dies

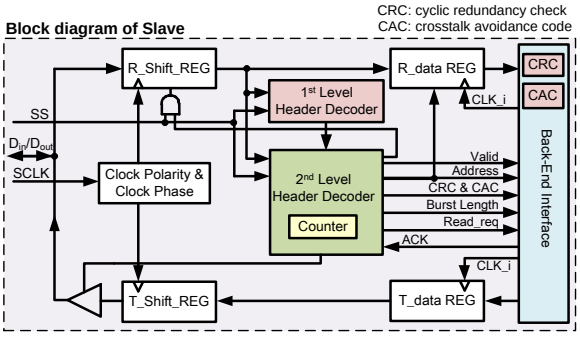

Fig. 4. Block diagram of slave module.

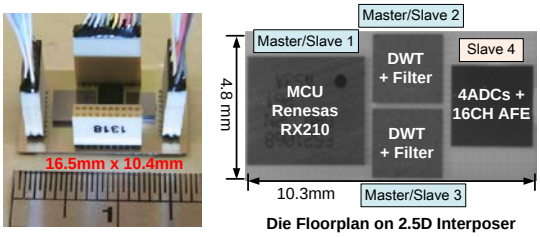

Fig. 5. 2.5D heterogeneously integrated bio-sensing microsystem.

by 2-layer RDL. The data width of this μ-SPI is defined as 4-bit with 1 SS pin and 1 SCLK pin. The supply voltage of all I/Os is 1.8V, and the frequency of μ-SPI is 100 kHz. The average power consumption of the proposed μ-SPI is only 23.2 μW measured by the power of I/Os. Accordingly, the power consumption of master/slave and slave modules is much smaller than the power of I/Os.

4. CONCLUSION

2.5D heterogeneous integrations provide efficient chip-to-chip communication via interposers. In this paper, an on-interposer bus, μ-SPI, is presented for providing low power inter-chip data communication in 2.5D integrations. The protocol of μ-SPI is designed by a hierarchical packetization technique to reduce the overhead of the header. The length of 1st level header is fixed for indicating the functionality of this packet. Based on the information of 1st level header, the 2nd level header is variable for providing wide range of the burst length, broadcasting selection and variable address. Moreover, a pseudo multi-master is proposed to replace the arbitration circuits via master passing. Only 1 master can exist by controlling MS_Flag in master/slave modules. The proposed μ-SPI is implemented in a 2.5D bio-sensing microsystem, and the average power of this on-interposer bus is only 23.2 μW at 1.8V and 100 KHz.

REFERENCES

[1] M. Motoyoshi, "Through-silicon via (TSV)," *IEEE Proceedings*, vol. 97, no. 1, pp.43-48, Jan. 2009.

[2] M. Koyanagi, T. Fukushima, and T. Tanaka, "High-density through silicon vias for 3-D LSIs," *IEEE Proceedings*, vol. 97 no. 1, pp. 49-59, Jan. 2009.

[3] R.-S. Cheng, et al., "Process characteristics of a 2.5D silicon module using embedded technology as a feasible solution for system integration and thinner form-factor," *IEEE Electronic Components and Technology Conference (ECTC)*, pp.1975-1979, 2013.

[4] J. H. Lau, "TSV Interposers: The Most Cost-Effective Integrator for 3D IC Integration," *Chip Scale Review*, Sept. 2011.

[5] Lattice Semiconductor Corporation, *Serial peripheral Interface*, RD1075, Revision 01.1, Dec. 2010.