Energy-Efficient Low-Noise 16-Channel Analog-Front-End Circuit for Bio-potential Acquisition

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***Abstract*—In this paper, an energy-efficient and low-noise 16-channel analog front-end (AFE) circuitry is proposed for acquisition of electrophysiological signals. This fully integrated front-end circuit comprises two differential difference amplifiers (DDAs) and DC offset rejection components. Additionally, the DDA is designed using a double input G_m-stage and a class-AB output for achieving high common-mode rejection ratio (CMRR), low-noise and energy efficiency. The 16-channel AFE with analog-to-digital converters (ADCs) is implemented in TSMC 0.18µm CMOS process. The measurement results show that the AFE can realize 60.3dB gain with only 20.67µW for each channel. The bandwidth of the AFE is from 2.32Hz to 6.61kHz. Furthermore, the total input referred noise and noise efficiency factor (NEF) are 0.826µV_{rms} and 2.78 only within the target frequency range of 0.1Hz to kHz, respectively.**

I. Introduction

In recent years, microsystems for bio-potential acquisition have been developed for neural sensing applications [1, 2]. Recording neural signals can help us to understand and identify diseases such as epilepsy and Parkinson's disease. However, the amplitude of these bio-potential signals is quite small in the order of few tens of µV to few tens of mV. Therefore, a low-power amplifier with low input referred noise is required for neural sensing applications. Furthermore, a high pass filter with the cut-off frequency around 1Hz should be introduced due to the interface between tissue and electrodes that causes a high DC offset for input signals. This DC offset has to be removed to prevent the saturation of amplifiers. Many designs of DC offset rejection components have been proposed using chopper stabilization [1] and MOS pseudo-resistors [2].

Although the chopper stabilization can achieve good noise performance and DC offset rejection, the large power consumption of the high chopper frequency is the critical design challenge. Additionally, the MOS pseudo-resistor is usually implemented by employing series of diode-connect MOS to achieve good trade-off between power consumption and performance. Therefore, an integrated neural amplifier comprised of differential difference amplifiers (DDAs) and pseudo resistors is presented in this paper. The DDA is designed to provide mismatch immunity, high common-mode rejection ratio (CMRR) and good amplification for neural sensing applications.

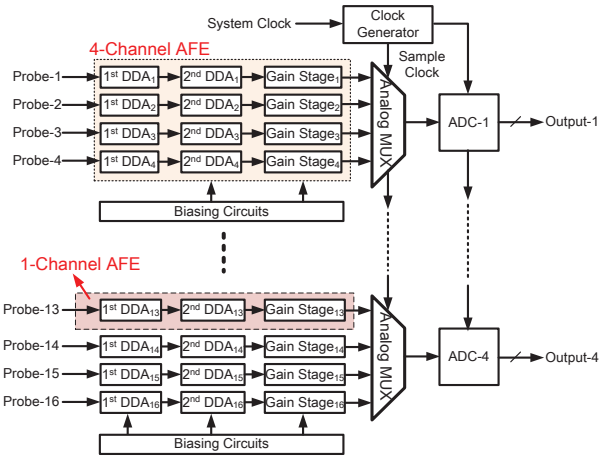

Fig. 1. 16-channel AFE with 4 ADCs for neural signal acquisition

II. Design of 16-Channel Neural Signal Acquisition

The microsystem for bio-potential acquisition is as shown in Fig. 1. Bio-signals are amplified by analog front-end (AFE) circuits and converted to digital codes by analog-to-digital converters (ADCs) [3]. Additionally, analog multiplexers with large output current are designed to select the corresponding signals to ADCs. A trade-off between power and area exists in the microsystem. The ratio between the number of AFEs and ADCs affects the overall performance. With the decreasing number of ADCs, the frequency of the system clock and output current of AFEs increases, and thus the power of system also increases significantly. For example, the output current of AFE in 16-channel AFE with one ADC would exceed 50µA for the required conversion rate. Based on the trade-off between power and area, 16-channel AFE with four ADCs are designed in the microsystem. The output current and the frequency of the switched clock of each analog multiplexer are 5µA and 8 kHz, respectively.

III. Design of 1-Channel AFE

1-channel AFE is composed of two amplification stages and one output stage for amplifying neural signals and

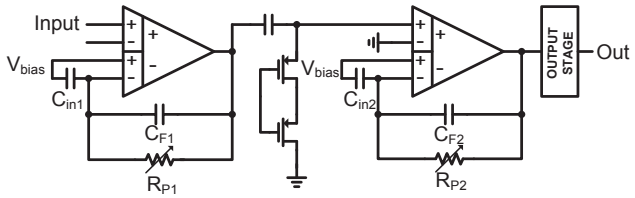

Fig. 2. Schematic of 1-Channel AFE.

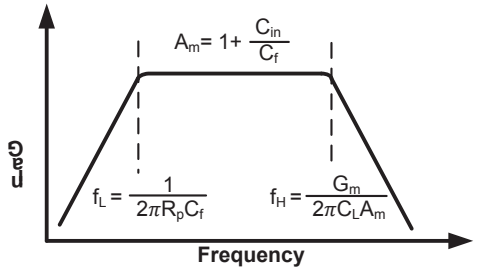

Fig. 3. Frequency response of DDA.

providing enough current to drive the following ADC. Fig. 2 presents the schematic of 1-channel AFE circuit with feedback capacitors and pseudo-resistors. The high-pass cut-off frequency is set by pseudo-resistor $R_{p1\text{-}p2}$ and feedback capacitors $C_{f1\text{-}f2}$.

Fig. 3 illustrates the frequency response of a DDA. The mid-band gain is determined by ratio of capacitors $1+C_{in}/C_f$, the low, and high cut-off frequency is approximately equal to $1/2\pi R_pC_f$, and $G_m/2\pi C_LA_m$, respectively. R_p represents the equivalent resistance of pseudo resistors. C_f and C_L are the feedback capacitor and loading capacitor, respectively. And A_m represents the current gain of the amplifier. To obtain the high-pass frequency around 1Hz, the time constant R_pC_f would be quite large. Therefore, pseudo resistors are utilized to provide large resistance without increasing the size of the capacitor for this high-pass frequency requirement.

A. 1st differential difference amplifier stage amplifier

The difference between a DDA and a differnitial amplifier is the number of input. A DDA is an amplifier with four input terminals which are noninverting port V_{pp}, V_{np} and inverting port V_{pn}, V_{nn}, respectively. The operation principle of a DDA can be described by four component vectors as (1).

$$\begin{bmatrix} 1 & -1 & -1 & 1 \\ 1/2 & 1/2 & 0 & 0 \\ 0 & 0 & 1/2 & 1/2 \\ 1/2 & -1/2 & 1/2 & -1/2 \end{bmatrix} \begin{bmatrix} V_{pp} \\ V_{pn} \\ V_{np} \\ V_{nn} \end{bmatrix} = \begin{bmatrix} V_D \\ V_{CP} \\ V_{CN} \\ V_{CD} \end{bmatrix} \quad (1)$$

The signal, V_D, is the differential voltage, and the other three signals, V_{CP}, V_{CP} and V_{CP} are the common-mode voltage which should be suppressed. Hence, the operation principle of a DDA can be represented in (2).

$$V_o = A[(V_{PP} - V_{PN}) - (V_{NP} - V_{NN})] \quad (2)$$

The ideal DDA amplifies the differential voltage by a nearly infinite amount, but fully suppresses all common-mode voltages. Generally, the major advantage of DDAs is that the input current is more than triple over that of the conventional differential amplifier. Therefore, the CMRR is dominated by the mismatch of the input stage, and can be improved by the symmetric layout and enlarging both the length and width of the input stage.

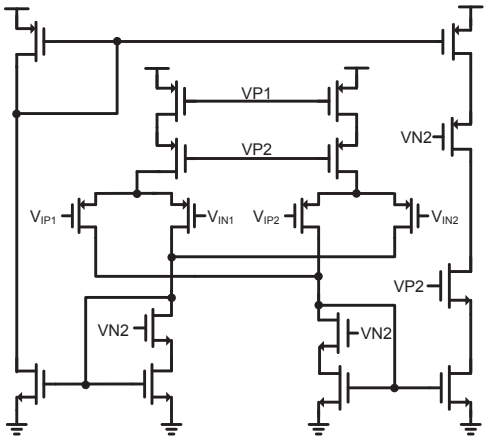

Fig. 4. Schematic of 1st DDA stage.

The schematic of the proposed first DDA stage is as shown in Fig. 4 with a DDA input stage, current mirrors, and a class AB output stage. The input voltage is converted to the current by the current mirror for controlling a class AB output stage. Additionally, the voltages of VP1, VP2, VN2, and VREF are generated by internal biasing circuits.

At low frequencies, the flicker noise will dominate the input signal. Therefore, the amplitude and resolution of the output signal will be limited by the flick noise. The model of flicker noise of DDA is as shown in (3).

$$V_n^2(f) = \frac{K}{C_{ox}WL}\frac{1}{f} \quad (3)$$

To reduce the power consumption and flicker noise of the DDA, the width of the PMOSs in the input stage is large. These PMOSs operate in the weak inversion or sub-threshold region to realize low power consumption, low flicker noise, and high voltage gain. The drain current of each input transistor is 0.5μA.

B. 2nd stage amplifier and output stage

In AFE design, increasing the cascaded stages induces large power consumption. At system-level, however, a conventional AFE with single stage design cannot achieve the optimal power efficiency [4]. The 1/2 LSB tracking error of ADC is modelled as in (4) where f_{3dB} and f_{max} represent the bandwidth of the amplifier and the maximum frequency of the input signal. Additionally, γ is the ratio of the holding time of each conversion cycle, and n is the resolution of ADC.

$$\frac{f_{3dB}}{f_{max}} > \frac{ln(2^n\pi\gamma)}{\pi(1-\gamma)} \quad (4)$$

For example, designing a single stage front-end amplifier and an ADC with 10-bit resolution (γ is set to 0.5) and 0.5 LSB of

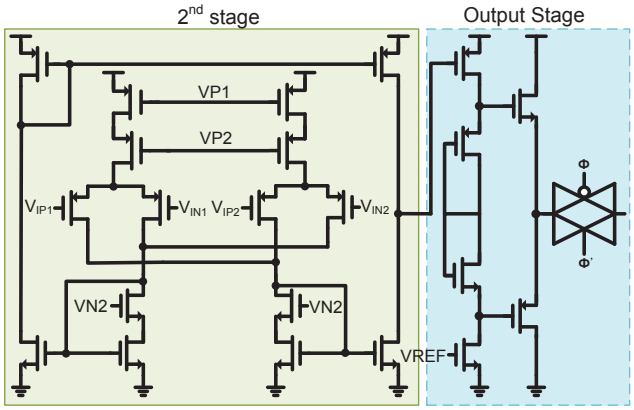

Fig. 5. Schematics of 2nd stage & output stage

tracking error for an input requires at least 5 times of f_{max} for the f_{3dB}. However, these parameters are hard to obtain in the design of bio-circuits. To achieve an acceptable conversion rate of the ADC with the corresponding low-pass cut-off frequency, f_{3dB}, the proposed AFE consists of two DDA stages and one output stage for optimizing the power efficiency. The circuitry of the 2nd stage is similar to that of the 1st stage. The voltage gain and current consumption of the 2nd stage is smaller than those of the 1st stage for energy efficiency.

The output stage is designed to provide large output current for driving the analog multiplexer which is connected to an ADC. The output stage consists of a common drain structure and a class AB output stage controlled by two diode-connected transistors for achieving large voltage swing. The output current is 5μA.

C. Modified pseudo resistor

A high-pass filter is designed to filter the DC offset from the input signal. Due to the limitation of the chip size, pseudo resistors are utilized widely in AFE designs. The equivalent resistance of pseudo resistors is large to provide a large time constant with an internal feedback capacitors for the small high-pass cut-off frequency. Many types of pseudo resistors have been proposed [5]. However, these pseudo resistors exhibit asymmetric and nonlinear resistance when the voltages across the pseudo resistors sweep from negative levels to positive levels. Furthermore, the drain-body junction of the pseudo resistor contributes leakage current in the order of pA and affects the performance of amplifiers. As such, the variation on the resistance of pseudo resistors and the distortion of the output signal both increase near the quiescent point.

The resistance of the conventional pseudo resistors cannot be higher than 100 GΩ due to the leakage current, even with ultra-low gate bias. Hence, the high-pass frequency is limited to around 100Hz, and some neural signals will be filtered. Therefore, a modified pseudo resistor with M1 is proposed to deal with the variation on the resistance as shown in Fig. 6. Fig. 7 presents the symmetric resistance property of different pseudo resistors. The modified pseudo resistor is a fully balanced pseudo resistor with higher resistance by connecting

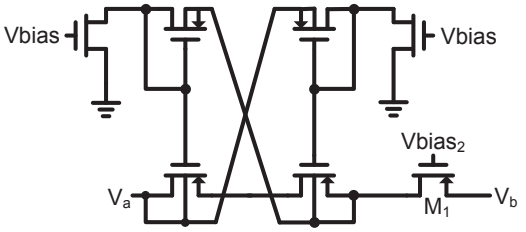

Fig. 6. Schematic of pseudo resistor with M1.

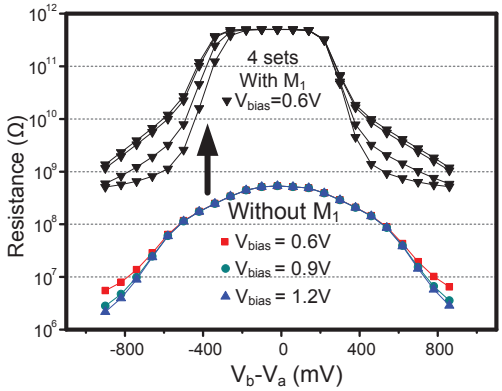

Fig. 7. Resistance of pseudo resistors with/without M1.

a serial transistor, M_1. The modified pseudo resistor with M_1 enhances the resistance. The Vbias and $Vbias_2$ are the fixed bias voltage generated by internal biasing circuitry

IV. Analysis of Power Efficiency with Noise

The performance of AFE is seriously degraded by the noises in the microsystem for bio-potential acquisition. The total input referred noise consists of flicker and thermal noises. The flick noise can be reduced effectively by increasing the size of the input stage. The formula of the thermal noise of a DDA is as shown in (5).

$$v_{thermal}^2 = \frac{32}{3}kT\left(\frac{1}{g_{mn}}\right) + \frac{16}{3}kT\left(\frac{g_{mn}}{g_{mp}}\right)^2\frac{1}{g_{mp}} \quad (5)$$

The g_{mn} and g_{mp} are the current gain of input stage and loaded transistors, respectively. The total input referred noise is a function of the temperature and the current gain of transistors. The current gain depends on the biasing current of transistors and the size of input transistors. Depending on the structure of a DDA, the current gain of the input stage is higher than that of an operational transconductance amplifier. Therefore, the total input referred nosie can be reduced effectively in the proposed AFE by utilizing the DDA structure and enlarging the symmetric input stage.

The total input referred noise is inversely proportional to the power of circuits. To minimum noises within the fixed power budget, a trade-off between power and noise exists. An important figure of merit (FOM) in AFE is the noise efficiency factor (NEF) as shown in (6) [6]. Based on (6), the NEF of the proposed AFE is 2.78.

$$\mathrm{NEF} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4KT \cdot BW}} \quad (6)$$

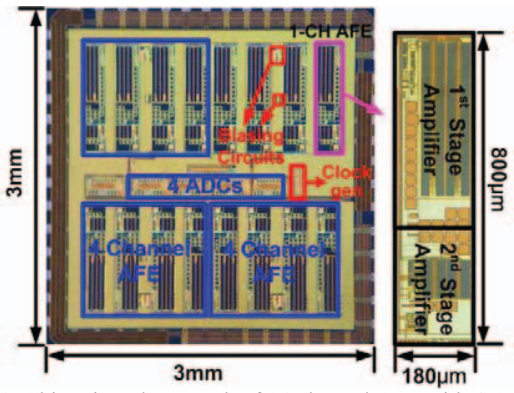

Fig. 8. Chip microphotograph of 16-channel AFE with 4 ADCs.

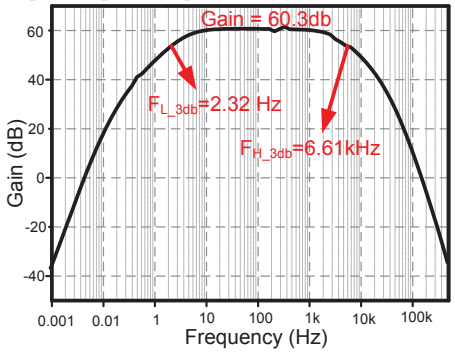

Fig. 9. Frequency response of 1-channel AFE.

V. Measurement Results

The proposed 16-channel AFE with 4 ADCs is fabricated in TSMC 0.18µm 1P6M CMOS process. The total area of the chip is 3mm x 3mm. the chip microphotograph is shown in Fig. 8. The active area of 1-channel AFE is 800µm x 180µm. Fig. 9 presents the frequency response of 1-channel AFE. The AFE provides a mid-band gain of 60.3dB with bandwidth from 2.32Hz to 6.61 kHz. A CMRR of 85dB and PSRR of 72dB are achieved to suppress the common mode noise from human bodies and power supply noise. Due to the high current gain and large area of the differential pairs in the 1st DDA stage, the total input referred noise is 0.826 μV_{rms} from 0.1Hz to 5 kHz. The comparisons between the proposed AFE and other similar amplifiers are listed in Table 1. The NEF of the proposed AFE is 2.78 only, close to the theoretical limit of 2.02 [8]. Fig. 10 presents the electroencephalography (EEG) signals before/after the proposed AFE.

VI. Conclusion

The design of 16-channel AFE is presented in this paper. 1-Channel AFE is composed of two stage DDAs and 1 output stage. A modified pseudo resistor is proposed to realize a high-pass filter with high resistance and to enhance the linearity of the AFE. Additionally, the AFE can realize 60.3dB gain with only 20.67µW for each channel. The bandwidth of the AFE is from 2.32Hz to 6.61kHz and the NEF is 2.87 only. With the features of low-noise and power efficiency, the proposed AFE design is useful for bio-potential acquisition.

TABLE. I. Comparison with other designs.

	[7]	[8]	[9]	This work
Technology	0.18µm CMOS	0.5µm CMOS	0.6µm CMOS	0.18µm CMOS
Power/channel	7.92µW	7.6µW	2.4µW	20.67µW
Gain	57.5 dB	40.85 dB	39.4 dB	60.3 dB
Bandwidth	10 Hz-7.2 kHz	45 Hz-5.32 kHz	0.36 Hz-1.3 kHz	2.32 Hz-6.61 kHz
Total input referred noise	3.5μV_{rms} 10 Hz to 100 kHz	3.06μV_{rms} 10 Hz to 98 kHz	3.07μV_{rms} 0.5 Hz to 30 kHz	0.826μV_{rms} 0.1 Hz to 5 kHz
NEF	3.35	2.67	3.09	2.78
CMRR	70.1 dB	>66 dB	>66 dB	> 82dB
PSRR	63.8 dB	>75 dB	>80 dB	60.08dB
THD	1%	1%	1%	0.98%

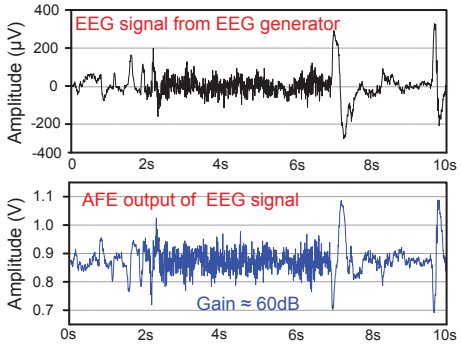

Fig. 10. (a) The original EEG signal (b) The output signal from ADC.

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