Recent Advances in ASIC-Compatible Circuit Techniques for a SOC in emerging new application areas (Invited Paper)

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Extended Abstract

In this paper, we review and present the latest advances in ASIC-compatible circuit techniques for newly emerging SOC areas, such as IOT and wearable computing devices. These applications require ubiquitous low-power consumption during a standby mode or when running low-intensity apps and a burst of high-performance for meeting the minimum performance requirement set by a system during a wakeup or communication state. Sub-threshold or near-threshold circuit techniques may provide a low-power solution. However, they have yet to demonstrate the remaining aspects of the SOC equation, such as performance, compatibility with ASIC tool sets and supporting ASIC design infrastructures.

Selective introduction of custom-circuit design techniques to an ASIC flow while ensuring the necessary compatibility has recently been proven as a very attractive alternative solution to the aforementioned problem. Extending the Dynamic-Voltage-Frequency Scaling (DVFS) range of an ASIC down to a Vccmin@circuit of 0.5 V and substantially smaller chip area and power have been achieved primarily by using four techniques: a pulse latch with an improved pulse generator, embedded SRAM operations with internal signals derived from the system clock in lieu of self-timed circuitry, reduced usage of transmission gates in favor of traditional stacked CMOS gates in critical standard cells, and restricted usage of cycle stealing during a SOC build.

In the presentation, we will cover the most recent advances in the four techniques in more detail with its power-performance-area (PPA) impact when applicable.