A 2kb Built-In Row-Controlled Dynamic Voltage Scaling Near-/Sub-Threshold FIFO memory for WBANs

Wei-Hung Du, Po-Tsang Huang, Ming-Hung Chang, and Wei Hwang, *Fellow, IEEE*

Department of Electronics Engineering & Institute of Electronics, and
Microelectronics and Information System Research Center (MIRC),
National Chiao Tung University, Hsin-Chu 300, Taiwan, R.O.C.

ABSTRACT

Due to the limited energy source, ultra-low power designs are significant approaches in energy-constrained SoCs. In this paper, a 2kb built-in row-controlled dynamic voltage scaling (DVS) FIFO memory is proposed to adopt the operation voltage in the near-/sub-threshold regions for the WBAN (wireless body area network) system. The row-based DVS provides the fine-grained power switch control for each sub-block. Therefore, the switching energy can be reduced, and the switching setup time can be eliminated. Moreover, only one sub-block are operated in the typical mode, and other sub-blocks are operated in the low-power mode and cut-off mode for realizing the power saving. Based on TSMC 65nm technology, the proposed DVS FIFO can achieve 47.8% power saving.

I. INTRODUCTION

Wireless body area network (WBAN) is a breakthrough personal healthcare technology for body condition monitoring and diagnosis. The WBAN system consists of a multiple of wireless sensor nodes (WSNs) and a central processing node (CPN) which are attached on human body skin and integrated in a portable device respectively as shown in Fig. 1 [1]. In a WSN sub-system for WBAN, the body signal from the external readout sensors are accumulated in the FIFO (first-in first-out) memory. The read/write clock frequency (625kHz/33kHz) and 16-bit resolution of the FIFO memory are based on the specification of the electrocardiogram (ECG) signal that requires almost the highest sampling rate and longest bit-length to represent its waveform among a human body. An analog to digital converter (ADC) with 16-bit resolution is used to sample body signals. Either of OFDM or MT-CDMA modulation scheme with 5MHz signal bandwidth can be used to transmit data. The read clock (*CLK_r*) frequency could run at 8 times slower for lower power consumption due to the processing and behavior of these modulation schemes.

Due to the limited energy source and long-term stability requirement for the WBAN system, robust ultra-low power designs are indispensable [1]. However, the FIFO memory dominates the total die area and power [2]. Accordingly, reducing power consumption of the FIFO memory is an urgent design consideration for optimal WBANs. On the other hand, voltage scaling is a popular method to reduce energy in digital circuit due to quadratic saving in the CV_{DD}^2 energy [3]. Thus, we proposed a 10T SRAM-based FIFO memory scaling down the supply voltage to the near-/sub-threshold region to achieve the minimum power consumption [4-5]. For further reducing the energy consumption in digital circuits, dynamic voltage scaling (DVS) techniques are utilized by adopting the system supply voltage depending on the performance requirement. [5-8]. Based on the DVS techniques, a lower voltage is applied to a circuitry in the low-power mode, while a nominal or boosted voltage is applied to a circuitry in the high-performance mode. Therefore, a 64 kb reconfigurable SRAM fabricated in 65 nm low-power CMOS process operating from 250 mV to 1.2 V was proposed in [7]. Additionally, for achieving the high reliability and high efficient power delivery in micro-power systems, a sub-threshold microcontroller with a power-efficient switched capacitor DC-DC converter was presented for the DVS SRAM [8].

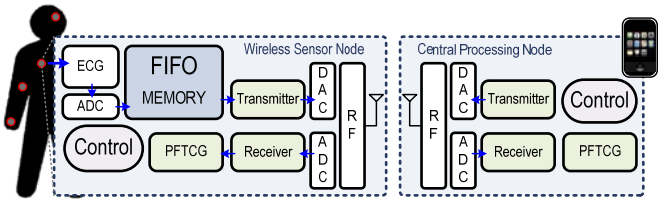

Fig. 1. Block diagram of WSN and CPN for WBAN.

In this paper, a 2kb built-in row-controlled DVS FIFO memory is proposed for WBANs using TSMC 65nm CMOS technology. A row-based adaptive power controller provides the fine-grained power switch control to adopt the supply voltage for the energy-constrained applications. The remainder of this paper is organized as follows. The proposed built-in row-controlled DVS FIFO memory is discussed in Section II. Section III and Section IV describes the row-based adaptive power controller and the DVS SRAM cells for the FIFO memory, respectively. Section V presents the simulation results, and the conclusion is given in Section VI.

II. BUILT-IN ROW-CONTROLLED DYNAMIC VOLTAGE SCALING (DVS) FIFO MEMORY

For a conventional DVS FIFO memory proposed in [5], while the FIFO switches the supply voltage from V_{DDH} to V_{DDL},or V_{DDL} to V_{DDH}, the switching setup time is required to avoid the supply shorting and the data corrupting due to the supply grid noise. Moreover, the significant charge/dischrage current induces large energy overhead during switching the supply voltage. With the increasing size of the FIFO, the switching setup time and switching energy are also increased. Therefore, a built-in row-controlled DVS FIFO memory is proposed to provide the fine-grained power switch through a row-based adaptive power switch controller. Based on the fine-grained adaptive power switch control, the switching energy can be reduced, and the switching setup time can be eliminated. Furthermore, the storage elements can be operated in V_{DDL} more often compared to those in the conventional DVS FIFO memory.

The built-in row-controlled DVS FIFO memory is composed of write peripheral circuitries, read peripheral circuitries, a row-based adaptive power controller, and SRAM based storage elements. Fig. 2 presents the block diagram of the proposed DVS FIFO memory, and these blocks are operated in different voltage levels, including 0.5V (V_{DDH}) and 0.3V(V_{DDL}). For generating dual supply voltage levels, the SC (switch capacitance) DC-DC converter is employed to decrease the voltage from the system voltage source instead of using

978-1-4577-2081-9/12/$26.00 ©2012 IEEE

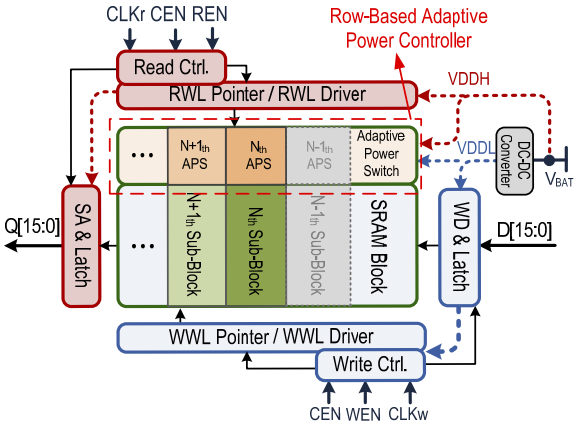

Fig. 2. block diagram of the built-in row-controlled DVS FIFO memory.

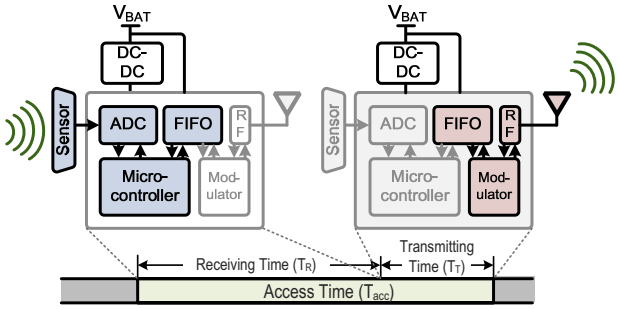

Fig. 3. The receiving time and transmitting time of FIFO in WBAN systems.

multiple voltage sources. Therefore, the V_{DDL} is generated by the (SC) DC-DC converter. The write peripheral circuitries consisting of write drivers (WD), a write pointer, write-word-line (WWL) driver, and write window controller are all operated at 0.3V. Additionally, the read peripheral circuitries composed of sensing amplifiers, a read pointer, read-word-line (RWL) drivers, and a read-window controller are operated at 0.5V. Both the read-window and write-window controllers are designed via read/write replica circuitries [4]. The row-based adaptive power controller is operated at both voltage levels, and provides the adaptive power switches for the storage elements.

The SRAM-based FIFO is divided into several sub-blocks for the fine-grained power switch control. In the read operations, the supply voltage of the active sub-block should be maintained at the high voltage level (0.5V) since the high accessing rate. In the write and data-retention operations, the supply voltage of SRAM sub-blocks can be scaled down to reduce the power consumption because of the low sampling rate. Therefore, each SRAM sub-block can be operated in three operating modes: ***Low-power mode***, ***Typical mode*** and ***Cut-off mode***. In the low-power mode, the FIFO records various physiological signals throughout its life time, e.g. heart rate and ECG or holds data. The voltage is scaling down to sub-threshold voltage (0.3V) for reducing the power consumption in the low simple rate. In the typical mode, the FIFO transmits the real-time informative cardiovascular parameters to a host. The voltage is kept at the near-threshold voltage (0.5V) for high accessing rate. After reading the data in the active sub-block, the data stored in the storage elements can be disturbed, and the supply voltage can be cut-off. Therefore, the supply voltage of inactive sub-blocks would be gated in the cut-off mode for leakage power minimization. Therefore, the supply voltage of cells is adopted between 0.3V, 0.5V and floating (cut-off) depending on the operation mode of the corresponding sub-block. Fig. 3 presents the receiving time (write operation at 33kHz) and the transmitting time (read operation at 625kHz) of the SRAM FIFO in

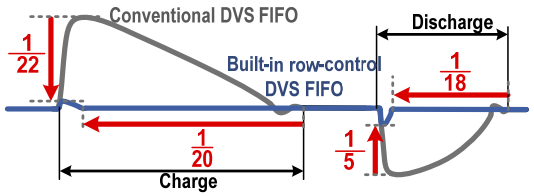

Fig. 4. The current waveform of the power switching.

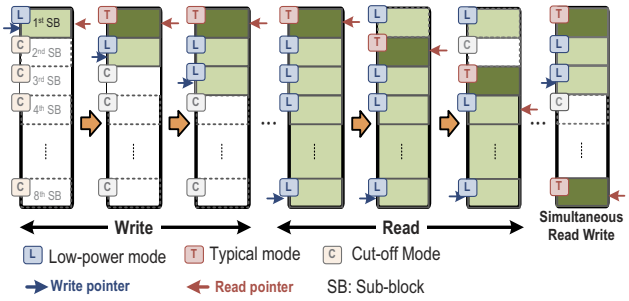

Fig. 5. Operation examples of the built-in row-controlled DVS FIFO.

the WBAN system. In the WBAN system, the SRAM sub-blocks are almost operated in the low power mode. According to this low-power mode dominated scenario, the supply voltage is scaled down into the sub-threshold region (0.3V) in the low-power mode to provide quadratic savings in active CV_{DD}^2 energy.

The proposed row-based adaptive power controller provides the fine-grained power switch control to the FIFO memory via adaptive power switches (APSs). Each sub-block contains an APS for adopting the voltage levels of this sub-block. Therefore, the row-based adaptive power controller generates the supply voltages along with the circular shifting read/write pointer. Based on the behavior of the FIFO, the status of each sub-block can be predictable. In view of this, the switching setup time for converting the supply voltage of a sub-block can be eliminated. Moreover, the capacitance of the supply voltage in a sub-block is much small than that of the whole FIFO memory. Thus, the switching setup time and switching power are smaller than that of the conventional DVS FIFO. Compared to the conventional DVS FIFO, the proposed built-in row-control DVS FIFO can reduce the charge current and the discharge current by 22x and 5x as shown in Fig. 4, respectively.

The row-based adaptive power controller generator the power switching control signals for the sub-blocks individually. Fig. 5 presents the operation examples of the built-in row-controlled DVS FIFO memory. The light green blocks represent that these sub-blocks are operated in the low-power mode. In these light green blocks, only one sub-block is prepared to be written. Other sub-blocks contain the stored data. The dark green block represents this sub-block is operated in the typical mode to be read, and the white block means this sub-block is the cut-off mode without the stored data. At the beginning, the first sub-block is in the low-power mode and other sub-blocks are all in the cut-off mode. During the receiving time of the FIFO memory, when the last word of 1st sub-block is going to be written, the 2nd sub-block will be changed to the low-power mode. After all words in 1st sub-block are written completely, the 1st sub-block is changed to the typical mode for the read operations. During the transmitting time of the FIFO memory, as the last word of the 1st sub-block is going to be read, the 2nd sub-block will be changed to the typical mode. Until the last word of 2nd sub-block is read-out, the 2nd sub-block is altered to the cut-off mode. In view of this, only one sub-block is in the typical mode during the transmitting time. Other sub-blocks are in the low-power mode or cut-off mode for further power saving.

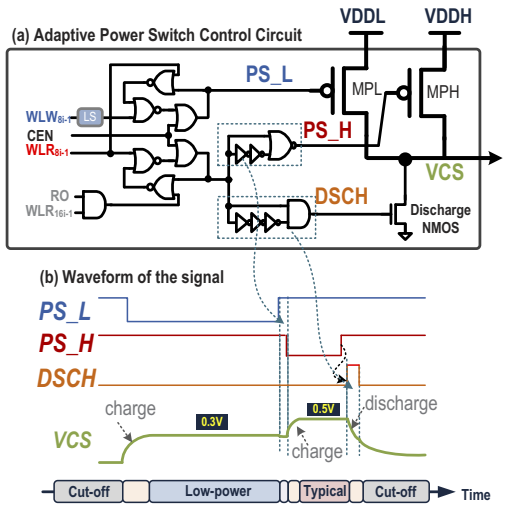

Fig. 6. Adaptive power switch unit and the corresponding waveform.

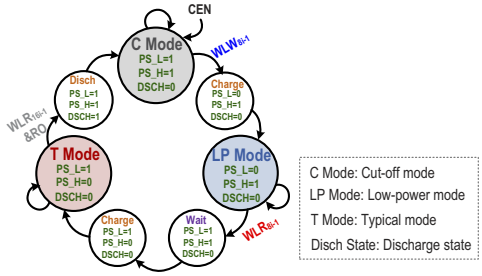

Fig. 7. FSM of the row-based adaptive power control.

III. ROW-BASED ADAPTIVE POWER CONTROLLER

The row-based adaptive power controller provides the fine-grained power switch control via adaptive power switches (APSs). The APSs is designed to adopt the supply voltage of a sub-block based on the three operation modes as shown in Fig. 6. The APS consists of two power PMOS, MPH and MPL, one discharge NMOS and the control circuitry. The APSs are controlled by the read/write pointer indicating the operation modes of the sub-blocks. The signals of read/write pointers (RWL/WWL) are decoded for the APSs to generate the power switch high (PS_H), power switch low (PS_L), and discharge (DSCH) via the control circuitry. The signal PS_H and PS_L are generated to control the MPH and MPL for providing V_{DDH}. and V_{DDL}, respectively. The DSCH is generated to control the discharge NMOS for the cut-off mode. The waveform of these signals is also shown in Fig. 6.

The finite state machine (FSM) for the corresponding control signals and the operation modes is as shown in Fig. 7. For supporting the reliability of the power switch, a wait state is inserted from the low power mode to the typical mode. A short path between two supplies exists while turning off MPL and turning on MPH simultaneously. For ensuring the security switch, a safe margin is added using the inverter delay line. Thus, the PS_H signal is delayed to guarantee the safe switch. Accordingly, when the operation mode is switched from the typical mode to the floating mode, a discharge state is inserted also. In the discharge state, the signal DSCH turns on the discharge NMOS to discharge the voltage level from V_{DDL} below to V_{DDL}. The discharge state is utilized to avoid the charge on the floating node (VCS) into the supply of V_{DDL}, if the MPL is turned on soon. Therefore, the delayed PS_H and the pulse of the DSCH can prevent the reverse current.

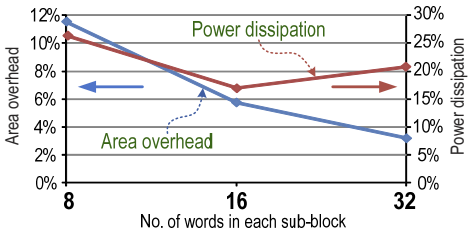

Fig. 8. The area overhead and power dissipation with different sub-block size.

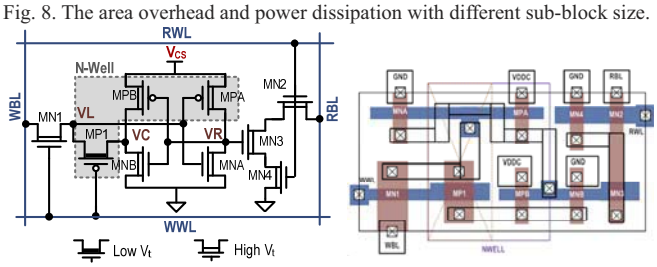

Fig. 9. Schematic and layout of the 9T SRAM bit-cell.

Table I. Corresponding control signals of the 9T SRAM bit-cell.

	V_{CS}	WWL	RWL	WBL	RBL
Hold	V_{DDL}	Gnd	Gnd	V_{DDL}	V_{DDH}
Read	V_{DDH}	Gnd	V_{DDH}	V_{DDL}	Floating
Write	V_{DDL}	V_{DDL}	Gnd	V_{DDL}/Gnd	V_{DDH}

To realize the maximum power saving, the appropriate size of each sub-block should be determined. The size of a sub-block is defined as the number of words in a sub-block. The major considerations for the size of a sub-block are the area overhead and the power dissipation. The area overhead is determined by the number of APSs and the size of power PMOSs. With the increasing size of the sub-block, the sizes of the power PMOSs are increased also. However, the number of the corresponding APSs is decreased. The power trade-off is determined by the power overhead (including the APSs and the switching power) and the power saving power in the low-power mode and cut-off mode. With the increasing size of the sub-block, the power overhead of APSs is decreased, but the switching power is increased. Furthermore, the power saving in low-power mode and the cut-off mode are not obvious in large sub-blocks because the granularity of the power switch is also decreased. Fig. 8 presents the area overhead and the power consumption in different sizes of a sub-block. While the size of each sub-block is 16-word, the power dissipation of the FIFO memory is the smallest one.

IV. DVS SRAM CELL FOR FIFO MEMORY

For achieving the high density and low power FIFO memory, the storage element of the proposed FIFO is composed of dual-port SRAM bit-cells. The dual-port SRAM bit-cells have independent read/write ports and read/write bit-lines. Therefore, a dual-V_T 9T SRAM cell is utilized in the FIFO memory as shown in Fig. 9. To simultaneously read/write different words at same time, the proposed 9T SRAM bit-cell have independent read/write bit-line (RBL/WBL). Moreover, the single bit-line scheme results in significant active power reduction [9]. Consequently, for reducing the leakage currents and enhancing the write margin and the SNM (static noise margin), both the dual-threshold CMOS (DTCMOS) and reverse short channel effect (RSCE) are utilized in the bit-cell [5]. The low V_t device (MP1) can improve the hold SNM and read SNM. In the sub-threshold region, the long channel length can release the process variation and improve $I_{on/off}$ ratio. According to the characteristic of the DVS FIFO memory, V_{CS} under the hold/read/write operations are V_{DDL}/V_{DDH}/V_{DDL}, respectively. Therefore, the corresponding control signals for the 9T SRAM bit-cell are list in Table I.

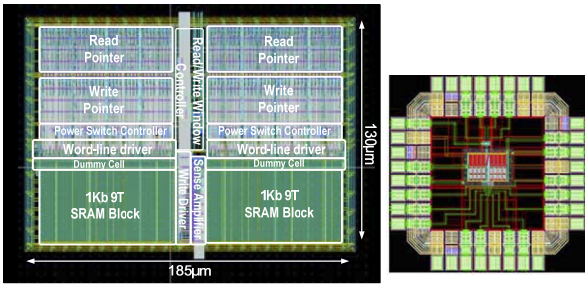

Fig. 10. Floorplanning and the layout view of the proposed FIFO memory.

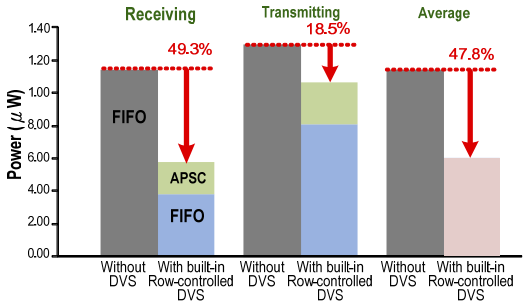

Fig. 11. Comparisons of the power consumption with/without the built-in row-controlled DVStechniqe.

Table II. The design profile of the built-in row-controlled DVS FIFO

Technology	TSMC 65nm CMOS technology
Supply Voltage	0.3V & 0.5V
Memory Size	2kb
Max Read/Write Frequency	6.4MHz/42.4kHz (@SS corner -20°C VDD±10%)
Read/Write Frequency	625kHz/33kHz
Operating Temp.	-20 ~ 80°C
Average Power (@TT, 25°C)	0.606μW
Leakage Power (@TT, 25°C)	0.529μW
Core Area	185μm x 130μm

The regular layout of the 9T SRAM bit-cell is design in "straight line layout" and "thin cell layout" as shown in Fig. 9. The straight line layout can facilitate lithography and reduce sensitivity to overlay errors. The thin cell layout can decrease the bit-line length for reducing the equivalent RC value of bit-line. Additionally, three metal layers are routed in the bit-cell. VDDC, GND, WBL and RBL are routed in metal-2, and VDDC, GND, WWL and RWL are routed in metal-3. Another layout consideration of the 9T bit-cell is the body biasing of the PMOSs. If the body of PMOSs is biased at V_{CS}, the pitch of N-Well to N-Well will decrease the FIFO density. Therefore, the body of the PMOSs should be fixed at 0.3V or 0.5V. If the body of the PMOSs is biased at 0.5V, the reverse body bias (RBB) occurs in the write and hold operation. On the other hand, if the body of the PMOSs is biased at 0.3V, the forward body bias (FBB) occurs in the read operation. RBB induces tiny degradation in the write margin and hold SNM. The power consumption of 0.5V body bias is less than that of 0.3V body bias. Therefore, the body of PMOSs is biased at 0.5V in the 9T SRAM bit-cell.

V. SIMULATION RESULTS

In this section, a 2kb built-in row-controlled DVS FIFO memory is implemented in TSMC 65nm technology at 625kHz reading frequency and 33kHz writing frequency, tolerating -20°C to 80°C temperature variation. The floorplanning and the layout view of the proposed FIFO memory is as show in Fig. 10. The design profile is summarized in Table II. The proposed DVS FIFO memory has only 0.606μW average power consumption in average per read/write access. Fig. 11 presents the comparisons of the power reduction between the convention FIFO without DVS and the proposed FIFO with built-in row-controlled DVS technique. In the receiving time, the benefit of the proposed built-in row-controlled DVS FIFO memory is attributed to the quadratic savings in active CV_{DD}^2 energy, and result in 49.3% power saving with 17.3% power overhead of the row-based adaptive power switch control. In the transmitting time, the proposed DVS FIFO has 18.5% power saving, consequently. Based on the execution of the WBAN system, the proposed DVS FIFO can achieve 47.8% power saving in average.

VI. CONCLUSIONS

An energy-efficient built-in row-controlled DVS FIFO memory is presented for the WBAN system in this paper. A row-based adaptive power controller provides the fine-grained power switch control to adopt the supply voltages of each sub-block. The adaptive power switches convert two operating supply voltages, 0.5V and 0.3V, in the typical mode and the low-power mode, respectively. Based on the fine-grained power switch control, the switching energy can be reduced, and the switching setup time can be eliminated. Moreover, only one sub-block are operated in the typical mode, and other sub-blocks are operated in the low-power mode and cut-off mode for realizing the power saving. The proposed DVS FIFO can achieve 47.8% power saving. Therefore, the proposed built-in row-controlled DVS FIFO memory is energy-efficient for WBAN applications.

ACKNOWLEDGEMENTS

This work was supported by ICL, ITRI, Taiwan, R.O.C., under Grant 100-EC-17-A-05-01-0626. The authors would like to thank Ministry of Economic Affairs and Ministry of Education, Taiwan, R.O.C. for their support.

REFERENCES

[1] T.-W. Chen, et al., "A 0.5 V 4.85 Mbps dual-mode basedband transceiver with extended frequency calibration for biotelemetry applications," *IEEE J. of Solid-State Circuits,* Vol. 44, No. 11, pp. 2966-2976, Nov. 2009.

[2] N. Verma, "Analysis towards minimization of total SRAM energy over active and idle operating modes," *IEEE Trans. on VLSI Systems,* Vol. 19, No. 9, pp. 1695-1703, Sept. 2011.

[3] D. Markovic, et al., "Ultralow-power design in near-threshold region," *IEEE Proceedings,* vol. 98, no 2, pp. 237-252, Feb. 2010.

[4] W.-H. Du, et al., "An Energy-Efficient 10T SRAM-based FIFO Memory Operating in Near-/Sub-threshold Regions," *in Proc. of IEEE International SoC Conference*, pp. 221-225, Sept. 2011.

[5] Y.-T. Chiu, et al., "Subthreshold asynchronous FIFO memory for wireless body area networks (WBANs)," *in Proc. of Int. Symp. Medical Information and Communication Technology (ISMICT)*, Mar. 2010.

[6] A. P. Chandrakasan, et al., "Technologies for Ultradynamic Voltage Scaling", IEEE Proceedings, Vol. 98, Issue 2, Feb. 2010, pp. 191-214.

[7] M. E. Sinangil, et al., "A Reconfigurable 8T Ultra-Dynamic Voltage Scalable (U-DVS) SRAM in 65 nm CMOS", *IEEE J. of Solid-State Circuits*, Vol. 44, No. 11, pp. 3163-3173, Nov. 2009.

[8] J. Kwong, et al., "A 65nm Sub-Vt Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter," *IEEE J. of Solid-State Circuits*, Vol. 44, No. 1, pp. 115-126, Jan. 2009.

[9] M.-H. Tu, et al., "Single-ended Subthreshold SRAM with Asymmetrical Write/Read-Assist," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 57, No. 12, pp. 3039-3047, Dec. 2010.