A Two-Write and Two-Read Multi-Port SRAM with Shared Write Bit-Line Scheme and Selective Read Path for Low Power Operation

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This paper proposes a two-write and two-read (2W2R) bit-cell for a multi-port (MP) SRAM design to improve the static noise margin (SNM) and solve the write-disturb issues of nanoscale CMOS technologies. Using an additional Y-access MOS (column-direction access transistor), the 2W2R MP SRAM adopts a scheme of combining the row access transistor and sharing write bit-line with an adjacent bit cell. This scheme halves the write bit-line number and mitigates the write current consumption caused by pre-charging the bit-line to $V_{DD}$. This paper also proposes a selective read path structure for read operation. Replacing the ground connection in the read port with a virtual $V_{SS}$ controlled by a $Y$-select signal reduces read-port current consumption. Results show that the proposed design reduces both the write current and read current consumption by 30%, compared to the conventional MP structure, from 1.3 V to 0.6 V $V_{DD}$. The proposed 8 Kb 2W2R MP SRAM was fabricated on the test chip using TSMC 40 nm CMOS technology.

Keywords: Multi-Port, SRAM, Write-Disturb, Half-Select, Read Path.

1. INTRODUCTION

As CMOS technology continues to scale down to deep nanoscale nodes, the system-on-chip (SOC) design demands large-capacity-embedded SRAM to improve the speed and area performance. The SOC design also increases storage requirements. The most widely used element is single-port (SP) SRAM, which has one write/read port for activation and a random access feature. However, demands for additional multi-port (MP) or dual-port (DP) SRAM have increased recently because they enable the parallel operation of high-speed communication, video applications, and application to a register file in a high-performance microprocessor. A single-port SRAM cannot support these functions. Thus, SOC chips that employ multi-port or dual-port SRAM designs for parallel operations can improve efficiency.1–6

Because an SP SRAM has only one clock to activate word-line (WL) and access memory cells simultaneously, data access must be executed serially. A DP SRAM design has two independent clocks that can access two ports of memory cells separately and execute parallel read or write operations. Figure 1(a) shows the DP 8T bit-cell scheme. Although DP SRAM is convenient for accessing cells to read and write simultaneously, it also generates write/read-disturb issues during common row access. Researchers have developed many techniques to solve the disturb issue of synchronous DP SRAM.7–8 However, the disturbance issue remains in both synchronous and asynchronous DP SRAM applications. One study proposed a technique for detecting the worst $V_{min}$ in asynchronous clock operation.9 Using this method, the circuit can identify the worst bit of an array with write/read-disturb issues.

To solve the read-disturb issue, previous studies of 8T-SRAM cell with decoupled read-port connecting a single-ended bit-line (BL) have been proposed.10–11 The decoupled single-ended sensing 8T-SRAM (DS8T) read-port avoids charge sharing with the internal node of the 8T bit-cell when the read WL is activated. Therefore, it has the read-disturb free feature. However, the single-ended BL suffers reduced BL sensing margin at read operation from bit-line leakage and noise problem. In addition, the read speed is also slow because the single-ended BL needs to be full-rail logic for the followed gate to sense. Another study presented a zigzag 8T SRAM cell (ZST) with differential-ended read BL scheme.12 The ZST cell has a decoupled differential-ended read-port. It just needs a small-swing on read BL pair. Therefore, the ZST
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Fig. 1. The conventional dual-port and 2W2R multi-port SRAM cell. (a) DP 8T SRAM bit-cell. (b) MP 12T SRAM bit-cell.

A cell can improve read access time and save read current consumption. Both of the single-ended and the differential-ended read-port 8T cell scheme still suffers write-disturb issue. These 8T SRAM cells scheme need a write-back (WB) operation on the unselected columns to overcome write-half-select issue. Therefore, these schemes will consume additional current during write-back operation.

One cross-point 10T (CP10T) cell structure isolates bit-line and storage nodes by a column-direction-control transistor (Y-access MOS) to improve static noise margin (SNM). It requires both a row-access signal and a column-access signal to activate the selected bit-cell. With that Y-access MOS, the read SNM of the unselected bit-cells is almost same as the hold SNM and overcome the write-disturb issue. Because of the Y-access MOS, the CP10T bit-cell has an area overhead about 60% larger than that of DSST or ZST bit-cell. However the CP 10T bit-cell discussion is limited for a single-port SRAM function only. The write or read function cannot operate at the same time.

The conventional 2W2R multi-port (MP) 12T bit-cell is based on a DP 8T cell, which has two write-ports and adds two read-ports at each side. Figure 1(b) shows the conventional 2W2R MP 12T bit-cell scheme. One study presented a two-port 6T unit cell with shared read/write assist-transistors per word. This design can solve the read/write disturb issue and improve the static noise margin problem. However, all the bit cells of a word are non-interleaved, raising the concern of soft errors. Another new multi-port 8T SRAM architecture with near 1-read/1-write (1R1W) capability multi-port operation has been proposed. This architecture provides a local write-back within one sub-array, while the rest of the sub-arrays can still perform read operation. However, the near 1R1W multi-port operation has one limitation. Some range of row addresses is not available for read and write operation at the same time.

This paper proposes a method that involves adding a Y-access MOS to the bit cell to resolve the MP SRAM write-disturb issue during common row access. This design maintains the cells of unselected columns in a hold state by disabling Y-access MOS. Contrary to conventional MP SRAM, the write-disturb phenomenon does not occur in write-half-select cells. Furthermore, this paper proposes a scheme that connects adjacent cells and shares a write bit-line. This scheme halves the write bit-line number, thereby reducing the power consumption of the bit-line when pre-charging the write-half-select cells to $V_{DD}$.

This paper also presents a selective read path. The proposed MP SRAM can reduce read current consumption by replacing the ground connection in the read port with a virtual $V_{SS}$ controlled by a Y-select signal.

The rest of this paper is organized as follows. Section 2 presents the concern of the multi-port SRAM cell to access cells at the same row within an array. Section 3 presents the proposed MP cell and proves that it overcomes the SNM and write-disturb problems in write-half-select cells. This section also presents the layout of the two adjacent MP cells. Section 4 presents the proposed MP SRAM architecture, with descriptions of the data-aware negative virtual $V_{SS}$ (VVSS) generator scheme and the selective read path for low power read operation. Section 5 provides simulation results and a comparison of the performance of the proposed 2W2R MP and conventional MP SRAM in current consumption and access time delay. Section 6 presents a summary of the proposed technique and presents a conclusion.

2. Multi-Port Cell Concerns

Conventional multi-port SRAM design suffers write-disturb issues, when executing write operations with different ports at the same row. Figure 2 shows two adjacent bit cells. When the write-A port and Column 1 are selected, the bit cell with the same row in Column 0 becomes write-half-select. Meanwhile, writing “0” in Column 0 from B-port is difficult because the storage node is pre-charged to high through the activated write-A port word-line (WAWL). In this case, the bit cell in Column 0...
encounters a write-disturb issue. Conversely, when write-B port activates and Column 0 is selected, the bit cell in Column 1 at the same row becomes write-half-select. Meanwhile, writing “0” in Column 1 from A-port is difficult because the storage node is pre-charged to high through the activated write-B port word-line (WBWL). In this condition, the bit cell in Column 1 encounters the write-disturb issue.

In addition to the write-disturb issue, the write-half-select cell encounters a read static noise margin (RSNM) that is worse than the hold static noise margin (HSNM) issue. As Figure 2 shows, when the bit cell in Column 0 encounters a write-half-select issue, its storage node suffers disturbance noise from the bit-line pair, WABL0 and WABLB0, pre-charging to high, despite the write-B port being deactivated in Column 0. The RSNM degrades most when both write ports activate at the same row.

When a write-half-select (dummy read) occurs in the cell of an unselected column, the RSNM becomes worse than the HSNM (with the WL of both write-ports deactivated), as the butterfly curve in Figure 3 shows. For example, when the WL of the write-A-port is activated, the WABL and WABLB are pre-charged to high, disturbing the internal storage node. This in turn causes the RSNM to deteriorate, as shown by the orange butterfly curve in Figure 3. When both ports are activated, deterioration of the RSNM is the worst, as shown by the green butterfly curve in Figure 3.

3. THE PROPOSED 2W2R MULTI-PORT CELL

Figure 4(a) shows the proposed 2W2R Multi-Port 14T unit cell scheme. This scheme shares the write-access MOS, NAW, and NBW with the left adjacent cell. Unlike a conventional 2W2R MP cell with double-end write bit-lines, the proposed MP cell has only a single-end write bit-line. Therefore, it is necessary to insert a pair of cut-transistor PXC and NYC into the cross-coupled latch within a bit cell as shown in Figure 4(a). The two cut transistors can enhance write capability to the bit cell with a single-end write bit-line. In a conventional MP cell scheme, the X-direction access MOS (row direction control), NAW, and NBW connect the internal node Q to the WABL and WABLB of A-port and B-port, respectively. The proposed MP cell scheme adds Y-direction access MOS (column direction control) NAY and NBY between the X-direction write-access MOS and internal node. Figure 4(b) shows a scheme in which two adjacent MP 13T bit cells are connected. The adjacent cells in Column 0 and Column 1 are connected by Y-direction

![Diagram](image-url)
Fig. 4. The proposed 2W2R Multi-Port cell scheme. (a) The proposed MP 14T unit cell. (b) The adjacent two Multi-Port 13T bit-cells connecting scheme.

access MOS controlled by WAY0, WBY0, WAY1, and WBY1. These columns share two common X-direction write-access MOS controlled by WAX and WBX. The two write-port bit-lines WABL0 and WBBL0 can be shared between Column 0 and Column 1. Similarly, adjacent cells in Column 2 and column 3 share two write-port bit-lines WABL2 and WBBL2. Therefore, this design retains only even-numbered write-port bit-line pairs, and omits odd-numbered write-port bit-line pairs. This halves the total write-port bit-line number, compared to that of the conventional 2W2R cell array. Hence, reducing the pre-charging BL to the $V_{DD}$ current of write-port bit-lines mitigates the write current consumption.

3.1. Write Enhancement Control

Because the proposed MP cell is a single-end write bit-line scheme, it is possible to insert a pair of pass-gate transistors controlled by XCut and YCut to the cross-coupled inverters as shown in Figure 5(a). When the bit cell is selected to write data, the XCut and YCut turn off to cut the feedback loop of the cross-coupled inverters. This helps enhance the write capability. XCut is an OR function output that is controlled by WAX and WBX. When WAX or WBX is selected, XCut is deactivated to turn off the PMOS. YCut is a NOR function output that is controlled by WAY and WBY. When WAY or WBY is selected, YCut is deactivated to turn off the NMOS.

The virtual ground node VVSS is a further enhancement for write “1” capability. When the bit cell is selected to write data “1,” VVSS can pull down to a negative voltage level during a short write word-line-activated period. Because the “1” written from the write bit-line must pass through 2 series-connected NMOS, it suffers the NMOS $V_{t}$ voltage drop and may not flip the pull-down NMOS, NDR. However, if VVSS can pull down to a negative level, the $V_{gs}$ of NDR enlarges and successfully flips the storage node to “0.” If the column is to write “0”, non-selected or in read mode, its VVSS retains 0 V. Figure 5(b) shows the VVSS operations of the proposed MP 13T bit cell.
3.2. Write-Half-Select SNM Issue Overcome

Figure 6(a) shows the operations of the proposed four MP 13T bit cells, and Figure 6(b) shows the corresponding SNM distribution curves. The bit-cell Cell_W is the selected cell with the activated WAX0 and WAY1 to write data from the bit-line WABL0. Hence, X0Cut and Y1Cut are deactivated through the row-control and column-control logic, and WBX0 and WBY1 are non-selected. The right adjacent cell Cell_R is the write-half-select bit cell with WAY0, WBY0, and X0Cut deactivated. Therefore, Cell_R can be isolated from the write bit-lines, WABL0 and WBBL0, and kept in a nearly hold state. The cell below Cell_W named Cell_B is another write-half-select bit cell in the column direction with WAX1, WBX1, WAY0, and WBY1 deactivated. Therefore, Cell_B can be isolated from the write bit-lines, WABL0 and WBBL0, and kept in a complete hold state. Figure 6(b) shows SNM curves of Cell_R, Cell_B, and Cell_BR shown in Figure 6(a). The SNM curve of Cell_R nearly coincides with the Cell_BR HSNM curve. Thus, the bit-line disturbance noise of Cell_B is isolated because both column-direction-control signals WAY0 and WBY0 are deactivated. Similarly, the SNM curve of Cell_B nearly coincides with the Cell_BR HSNM curve. Therefore, the SNM degradation issue occurring in a conventional write-half-select cell can be overcome. The write-half-select SNM and HSNM curves shown in Figure 6(b) are 10000 Monte Carlo simulation results in 0.6 VDD, 25 °C, and FS corner.

3.3. Overcoming Write-Disturb Issue

Figure 7 shows a one-row diagram of connecting four proposed 2W2R MP cells in one row. When Cell_1 writes “0” from A-port bit-line WABL0 in Column 1, the B-port write bit-line WBLB0 is pre-charged to high. In this case, WAY0 and WBY0 are deactivated because Cell_0 is not selected for write operation, and the path to the storage node of Cell_0 is cut off. Therefore, Cell_0 maintains its hold state and avoids the write-disturb issue. If Cell_2 additionally writes “0” from B-port bit-line WBBL2 in Column 2 and Cell_3 is not selected for write operation, WAY3 and WBY3 are deactivated, and the path to the storage node of Cell_3 is cut off. Therefore, Cell_3 can be isolated because both column-direction-control signals WAY0 and WBY0 are deactivated. Similarly, the SNM curve of Cell_B nearly coincides with the Cell_BR HSNM curve. Thus, the bit-line disturbance noise of Cell_B is isolated because both row-direction-control signals WAX1 and WBX1 are deactivated. Therefore, the SNM degradation issue occurring in a conventional write-half-select cell can be overcome. The write-half-select SNM and HSNM curves shown in Figure 6(b) are 10000 Monte Carlo simulation results in 0.6 VDD, 25 °C, and FS corner.
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Fig. 6. (a) Cell_W is the write selected cell with WAX0 and WAY1 activated, but WBX0 and WBY1 deactivated. Cell_R is the right adjacent cell. Cell_B is the cell below Cell_W. Cell_BR is the row and column non-selected cell. (b) MP 13T cell SNM simulation results corresponding to (a) with 10000 MC. \( V_{DD} = 6 \) V, FS corner.

Proposed MP Cell HSNM

3.4. Layout Implementation

Figure 8(a) shows a scheme connecting two adjacent MP 13T cells of Columns 0 and 1, and Figure 8(b) shows their corresponding layout graph. This two-cell scheme demonstrates bit-line number reduction, which can also mitigate bit-line and word-line capacitance. Columns 0 and 1 share the write bit-lines WABL0 and WBBL0, as required by the scheme shown in Figure 8(a). This approach halves the number of bit-lines. Columns 0 and 1 also share the write-access pass-gates, NAW and NBW, further reducing the gate capacitance of the write word-line

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control signal and the write bit-line junction capacitance. In conventional MP 12T cells, WAWL/WBWL connects to both WABL0/WBBL0 and WABL0/WBBL0 separately. Therefore, the proposed design further reduces the WL gate capacitance of the MP 13T scheme. The layout area of MP 13T cells is 2.786 $\mu$m$^2$, as Figure 8(b) shows.

Because it contains a write-enhancement control, the proposed MP cell layout requires some area for the two transistors PXC and NYC. Compared with the conventional MP cell layout, the proposed layout has an area overhead of approximately 10.9%.

4. 2W2R MULTI-PORT SRAM ARCHITECTURE

Figure 9 shows the proposed 8 Kb 2W2R multi-port SRAM architecture. The 8 Kb SRAM chip consists of two banks. Each bank contains 4 Kb capacity with 64 rows and 64 columns. The multi-port SRAM contains two write ports, write-A port and write-B port, on the top part. It also contains two read ports, read-A port and read-B port, on the bottom part. Each write port has nine address bits as WA[8:0] and WB[8:0]. Each read port has nine address bits as RA[8:0] and RB[8:0]. Each write port contains 16 input bits as DA[15:0] and DB[15:0]. Each read port contains 16 output bits as QA[15:0] and QB[15:0].

Every time the multi-port attempts to write data to a cell, the A/B-port data must first enter a write buffer. Next, the data pass through write-Y interleaved 8-to-1 MUX and select one of the write BLs, WABL/WBBL from eight bit-lines. The data on the write BL can be written into the selected bit cell after activating the corresponding write word-line WAX/WBX and write \( Y \)-select signal WAY/WBY.

Similarly, when the multi-port attempts to read data from a cell, the A/B-port data must first be read on the bit-line RABL/RBBL. The data then pass through read-Y interleaved 8-to-1 MUX and are sent to the output buffer.

4.1. Data-Aware Negative VVSS Generator Scheme

Figure 10(a) shows the data-aware negative VVSS generator scheme. In a write cycle, when A/B-port input data DATA_A/DATA_B are “1,” the PMOS capacitor is boosted to a negative voltage level. Once WAY/WBY is activated, the negative voltage passes through 8-to-1 MUX to the selected VVSS line. Figure 10(b) presents the negative voltage.
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Fig. 8. (a) The adjacent two MP cells scheme. (b) The corresponding layout of two MP 13T cells.

VVSS level versus $V_{DD}$. Figure 10(c) shows the write margin comparison between conventional MP and the proposed MP cell with write enhancement control. The definition of write margin is the ratio of the write BL voltage divided by $V_{DD}$ level when the cell’s storage node flipped. With write enhancement control, the write margin of the proposed MP cell can be very close to that of conventional MP cell at 0.6 V $V_{DD}$.

4.2. The Selective Read Path Scheme

Except for the write current reduction, the read current reduction replaces the read-port ground connection with RA VS and RBVS as shown in Figure 11(a). Although this technique was not implemented on the test chip, this paper still proposes the selective read path scheme shown in Figure 11(b) for read current reduction. When the column-direction control signal RAY[0] is activated, it controls RA VS[0] to 0 V. Conversely, because RAY[7] is deactivated, RAVS[7] becomes the $V_{DD}$ level. The selective read path sets the selected read-port RA VS to 0 V and sets the other unselected RA VS lines to the $V_{DD}$ level. Thus, only the selected BL can discharge from $V_{DD}$ to ground when the storage node is “1” and the other BLs cannot discharge. Therefore the unselected BLs can return the read-half-select current consumption of pre-charging back to $V_{DD}$. Additionally, a replica column tracks the read-BL (RBL) to control the timing of pre-charging the RDL line and the latch output to Q. The proposed bit-interleaving design selects only one of eight RBLs, achieving a 30% reduction in read current per read port.

5. SIMULATION RESULTS AND PERFORMANCE COMPARISON

The proposed MP SRAM architecture takes advantage of sharing a write bit-line across WL-access MOS between...
adjacent columns, thereby reducing the number of write bit-lines. The effect of a reduced bit-line number on the current consumption was verified when the bit-lines were pre-charged back to $V_{DD}$. Figure 12(a) shows the write current reduction ratio between the proposed MP and conventional MP. Additionally, the selective read path scheme discharges only one RBL and the other seven RBLs remain in the pull-high state, reducing the read current. Figure 12(b) shows the read current reduction ratio between the selective read path and the conventional ground connection.

The proposed design adds a $Y$-access MOS between the internal node and the write WL-access transistor, thus affecting the write-access time. The series resistance of the $Y$-access MOS and write WL-access transistor raises the access time delay from 0.5% to 3%. The selective read path employs a $Y$-direction signal to control the read-port connection determined by an inverter output instead of connecting to ground directly. Therefore, the read access time increases from 2% to 4%. Figure 12(c) shows the write access time delay ratio. Figure 12(d) shows the read access time delay ratio.

Figure 13(a) shows a diagram of the proposed MP-adjacent cells in the hold state. WAX, WBX, WAY, and WBY are deactivated when the write BL is pre-charged to $V_{DD}$. Because the write BL leakage current must pass through two disabled series-connecting MOS to the “0” storage node, this design reduces the sub-threshold leakage compared to that of the conventional MP cell array, which has only one write WL-control MOS on the leakage path. Figure 13(b) shows a write BL leakage reduction ratio of approximately 60% to 90%. Figure 13(a) shows the selective read path pulled high to read ports on RAVS/RBVS, reducing the read BL leakage current. Figure 13(c) shows the read BL leakage reduction ratio more than 40%.
This paper includes a simulation test of write/read A/B-port operations executed at the same row. The A-port activates Column 0 and executes write/read operations for five continuous cycles, as Figure 14(a) shows. The B-port activates Column 7 and also executes write/read operations. The data in the Figure 14(b) waveform indicate that the internal node of the 2W2R MP cell can be written and read as required. Figure 15 shows a photo of the 40 nm 2W2R 8 Kb multi-port SRAM. The test chip area is 0.9701 mm².

Table I shows the multi-port SRAM comparison with related works. For four table entries, i.e., write-disturb issue, SRAM macro area (including cell array and SRAM periphery circuit), operational frequency, and power consumption, the comparison criterion is based on 2W2R capability. In write-disturb comparison, only this work and ISQED14 are free of write-disturb issue, but the structure in Ref. [14] is not a bit-interleaving structure, still raising soft-error concern. In SRAM macro area comparison, this
Fig. 12. (a) The write current reduction ratio between proposed MP and conventional one. (b) The read current reduction ratio between proposed MP and conventional one. (c) The write access time difference between proposed MP and conventional MP structure. (d) The read access time difference between proposed MP and conventional MP structure.

Fig. 13. (a) The proposed MP cell BL in a hold state. (b) The write BL leakage reduction ratio of proposed MP versus conventional MP. (c) The read BL leakage reduction ratio of proposed MP versus conventional MP.
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Fig. 14. (a) The MP A/B-port write/read simulation pattern test at the same row. (b) The corresponding A/B-port cell waveform.

Fig. 15. The chip photo of the 40 nm 2W2R 8 Kb multi-port SRAM.
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Table I. The Multi-Port SRAM comparison with related works.

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6. CONCLUSION

This paper presents design techniques to improve the write and read-low-power capabilities of a 2W2R 8 Kb multi-port SRAM. The test chip was fabricated using a TSMC 40 nm CMOS technology. The test chip area is 0.9701 mm². The MP cell proposed in this paper can prevent the write-disturb issue in write-half-select cells during common row access. The proposed design overcomes this problem by adding a column-direction MOS to disable access from the write bit-line to the internal node. The shared write-bit-line scheme halves the write-bit-line number and reduces the write current consumption by 30%. The proposed selective read path can also maintain the unselected read-port bit-lines at the pre-charged high level. Therefore, the read current consumption is reduced by more than 30%. In comparison with other related works, this work has the optimum area overhead and power saving based on same clock frequency.

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References


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