An Energy-Efficient Level Converter with High Thermal Variation Immunity for Sub-threshold to Super-threshold Operation

Mei-Wei Chen[1], Ming-Hung Chang[1], Yuan-Hua Chu[2], and Wei Hwang[1]

[1]Dept. of Electronics Eng. & Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan
[2]Information and Comm. Research Lab., Industrial Technology Research Institute, Hsin-Chu, Taiwan
tako.ee88g@nctu.edu.tw

ABSTRACT

A multiple supply voltage scheme is an emerging approach to reduce power dissipation. The scheme requires a level converter as a bridge for different voltage domains. Conventional level converters fail to work in sub-threshold region due to the pull-down devices and the pull-up devices operate in sub-threshold and super-threshold region respectively. By employing diode-connected PMOS transistors, multiple-threshold-voltage CMOS (MTCMOS), and stack leakage reduction techniques, the proposed cross-coupled level converter achieves small propagation delay, low power consumption, and best power-delay-product (PDP) performance. Also, the reverse short channel effect is utilized to provide our level converter better process/thermal variation immunity. We also propose a dual edge-triggered explicit-pulsed level-converting flip flop (LCFF) concept combining a DCVSPG latch and our level converter. The proposed cross-coupled level converter is designed using TSMC 65nm bulk CMOS technology. It functions correctly across all process corners for a wide input voltage range, from 150mV to 1V. The level converter has a propagation delay of 52ns and a power dissipation of 21nW when the input voltage is 150mV.

I. INTRODUCTION

Power dissipation becomes a critical concern in emerging portable applications such as biological systems or wireless electronics. Constrained by a small form factor, the battery lifetime is a critical challenge. Ultra-low voltage design has been proofed to be an effective solution since supply voltage is quadratic function of energy. However, the side effect of scaling down the supply voltage is the degradation of performance and robustness. Multiple supply voltage techniques have been presented for low power design [1]. Some parts of a digital system are employed a nominal supply voltage to meet the performance needs. The other parts are operated in the sub-threshold region to save the power dissipation. Such multiple voltage designs can run different blocks at the different supply voltages to perform dynamic voltage and frequency scaling (DVFS) on different voltage domains. Between the two different voltage domains, it may occur a situation that a lower supply voltage gate drives a higher supply voltage gate. While the high output of a lower supply voltage gate is not strong enough to fully turn off a PMOS gate supplied by a higher supply voltage, this results in a DC leakage path from the voltage source to the ground and increases the power dissipation. In addition, if a higher supply voltage gate is driven by a lower supply voltage gate, it cannot have a full output swing and causes a function error. To solve these problems, a level converter is essentially inserted at the interface between two different voltage domains. Nonetheless, the level converter also consumes power and causes a considerable timing delay. In the multiple supply voltage systems, it is crucial to design a high-speed and energy-efficient level converter.

Fig. 1(a) shows a conventional level converter. Two cross-coupled PMOS transistors form a positive feedback loop to make the output full swing. However, the cross-coupled level converter encounters an imbalance driving strength problem so that the positive feedback can't be triggered. For the signal converting from sub-threshold to super-threshold, some transistors of the level converter are operated in the sub-threshold region and the other transistors perform in the super-threshold operation. A Monte Carlo simulation of the conduction current in 65nm CMOS technology is shown in Fig. 1(b). It demonstrates that the driving ability of super-threshold PMOS is much

978-1-4673-1295-0/12/$31.00 ©2012 IEEE

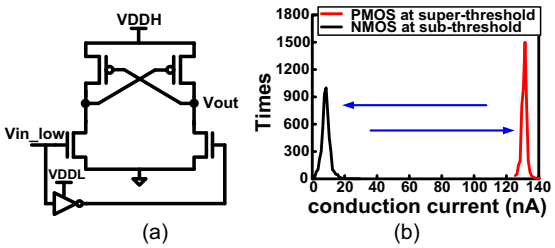


Figure 1: (a) conventional level converter (b) Monte Carlo simulation of conduction current

larger than sub-threshold NMOS. Such driving ability difference leads to a level converter failure. Recently, many level converters [2]-[10] have been designed to operate in the sub-threshold region. In [2], the cross-coupled PMOS transistors are connected by two diode PMOS transistors. They can reduce the pull-up devices driving ability to enable sub-threshold operation. There is a short current problem occurred in [2] resulting large power dissipation. A level converter with a short current limiting technique was presented in [3]. It inserted two NMOS transistors in the positive feedback loop between the latch PMOS transistors and the PMOS diodes. The two NMOS transistors speed up the transition to avoid a short current path. However, the reliability of two NMOS transistors is susceptible to the variations. In [4], it cascaded two conventional cross-coupled level converters to prevent the short current path. Nevertheless, the cascaded architecture results in a slow propagation speed at higher supply voltage.

In this paper, we propose a power-delay-product optimized and robust level converter with high thermal variation immunity for sub-threshold to super-threshold operation. This paper is organized as follows. Diode-connected PMOS transistors, multiple-threshold-voltage CMOS, and stack leakage reduction techniques are discussed. Also, reverse short channel effect and inner inverter device sizing are analyzed in Section II. The simulation results of this work under TSMC 65nm CMOS technology are proposed in Section III. Finally, Section IV concludes this work.

II. PROPOSED ENERGY-EFFICIENT LEVEL CONVERTER WITH HIGH THERMAL VARIATION IMMUNITY

The schematic view of the proposed level converter is shown in Fig. 2. It is based on the cross-coupled level converter and adapts two diode-connected PMOS transistors in [5]. The

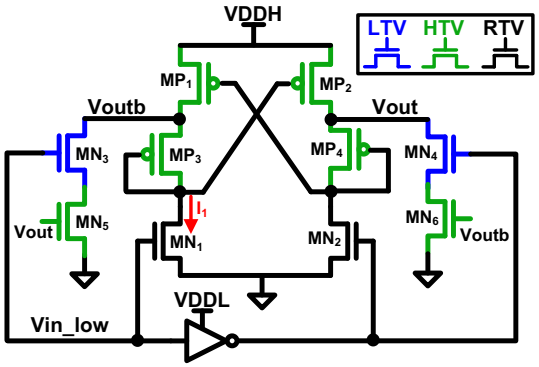


Figure 2: Schematic view of the proposed level converter

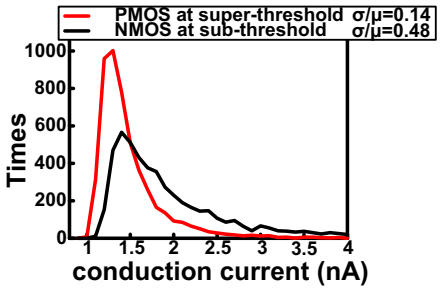
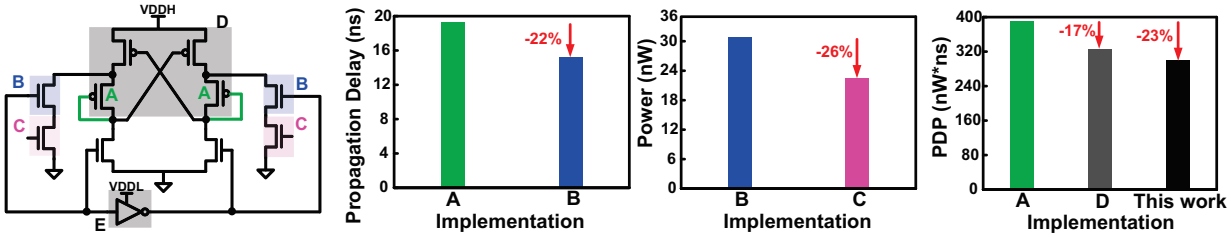


Figure 3: Monte Carlo simulation of conduction current of two diode-connected PMOS transistors

multiple-threshold-voltage CMOS design is also employed in the proposed level converter. In addition, a stack leakage reduction technique is used to reduce the power consumption. Reverse short channel effect is also exploited to make the proposed level converter more reliable and robust across all the process corners and temperature variations.

A. Diode-connected PMOS transistors

From Fig. 1(b), we can find that the conventional level converter has an imbalance driving ability problem when converting a signal from the sub-threshold region to the super-threshold region. For TSMC 65nm CMOS technology, the ratio of pull-down device (NMOS) and pull-up device (PMOS) should be larger than 200X so that the conventional level converter can barely be operated at an input supply voltage of 200mV. The resulting width of NMOS causes a huge area overhead. In Fig. 2, the proposed level converter utilizes diode-connected PMOS transistors to reduce the pull-up driving ability [5], MP_3 and MP_4 serve as a current limiter. Two PMOS diodes maintain its initial value during the transition. The initial value is equal to a small diode voltage drop and limits the PMOS strength. As a result, the pull-down devices, MN_1 and MN_2, can



(a) (b) (c) (d)

Figure 4: (a) A: two diode-connected PMOS. B: multi-V_{th} devices. C: leakage reduction technique. D: reverse short channel effect. E: inner inverter sizing. (b) By implementation B, delay reduction up to 22% (c) By implement C, power reduction up to 26% (d)By implement D, PDP reduction up to 17%. Finally, combining all implementation, overall PDP reduction up to 23%

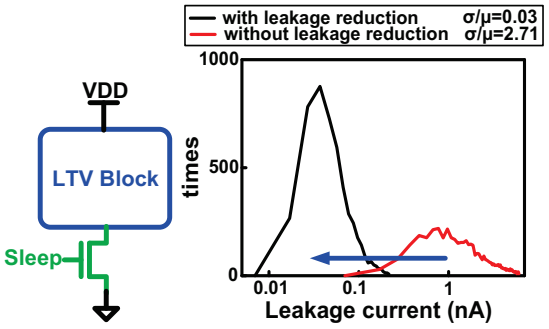
sink the I_1 current even when the circuit is operated in the sub-threshold region. Comparing the results in Fig. 1(b) and Fig. 3, the PMOS conduction current is decreased dramatically and closer to the NMOS conduction current. Thus, they have a comparable driving ability. By connecting two PMOS diodes, the modified cross-coupled level converter overcomes the imbalance conduction current problem when operated at low voltage. Thus, the proposed level converter can convert the signal from sub-threshold region to super-threshold region successfully.

B. Multiple-threshold-voltage CMOS (MTCMOS)

The MTCMOS design is usually provided in the modern technology. Low-threshold voltage (LTV) devices take the advantage of the speed but have a severe leakage current problem. High-threshold voltage (HTV) devices have a less leakage current but sacrifice the speed. There is a trade-off between the propagation delay and the power consumption. Therefore, power-delay-product (PDP) should be used as a figure of merit for level converter analysis. To further weaken the PMOS strength, MP_1, MP_2, MP_3, and MP_4, use the HTV devices. To enhance the NMOS strength, MN_1, MN_2, MN_3, and MN_4, are considered using the LTV devices. If all the NMOS transistors are utilized the LTV devices, the power consumption will be increased very much. In the proposed level converter, only MN_3 and MN_4 use the LTV devices. This configuration can make a faster speed when output changes from high to low and improve the total propagation delay time. From Fig. 4(b), we can find that the propagation delay is reduced up to 22%.

C. Stack Leakage reduction technique

The leakage current causes the static power consumption. With the scaling down technology, this problem becomes severely in the LTV logic



(a) (b)

Figure 5: (a) leakage reduction technique [11] (b) Monte Carlo simulation of leakage current with/without leakage reduction technique

block. In Fig. 5(a), the LTV block is connected by a HTV NMOS transistor [11]. When the LTV block is in a sleep mode, the connected HTV transistor is also turned off by a sleep signal to avoid a leakage path to the ground. A sleep mode means the block function is turned off. From the Monte Carlo simulation in Fig. 5(b), the leakage current is reduced quietly a lot when using the leakage reduction technique. This technique is adapted in the proposed level converter. MN_3 and MN_4 are the LTV devices, they are connected by the HTV NMOS transistors, MN_5 and MN_6, as shown in Fig. 2. The signal of *Vout* and *Voutb* are feedback to control MN_5 and MN_6 adaptively. When the input is "1", MN_3 is in an active mode and MN_4 is in a sleep mode. *Vout* is charged by MP_2 and turns on MN_5, so the left branch works as usual. *Voutb* is discharged by the MN_1 and turns off MN_6. The right branch is in a sleep mode. When the input is "0", *Vout* turns off MN_5 and *Voutb* turns on MN_6. The left branch is in a sleep mode and the right branch works as usual. In both of the situations, there are no leakage path existing. Fig. 4(c) shows that the power consumption can be reduced up to 26% by using the modified leakage reduction technique.

D. *Reverse short channel effect*

The minimum channel length is typically selected for the optimal speed and power performance in the super-threshold operation since the short channel effect is a dominant factor. However, there is a different scenario in the sub-threshold region. Because of the significantly reduced drain-induced-barrier-lowering (DIBL), the reverse short channel effect becomes a major factor in the sub-threshold operation. Due to the reverse short channel effect, the threshold voltage decreases monotonically and the conducting current increases exponentially when the channel length is longer. Thus, the best PMOS channel length of the proposed level converter is not the minimum length. Based on the simulation data, the optimal device sizing is 85nm in this work. While the channel length is longer than the optimal length, the reverse short channel effect is weak. By taking advantage of the reverse short channel effect, the PDP value can be decreased 17%, as shown in Fig. 4(d).

E. *Inner inverter device sizing*

In the proposed level converter, there is an inner inverter responsible for providing the differential input. Its supply voltage level is as the same as the input signal voltage level. Therefore, the inner inverter is also operated in the sub-threshold region and causes a propagation delay time. As Fig. 2 shown, MN_2 and MN_4 are controlled by the output of the inner inverter. The positive feedback loop has to wait for MN_2 and MN_4 settling down to be triggered. However, the faster speed brings larger power consumption. Therefore, there is a trade-off between delay and power.

F. *Proposed level converter performance*

Combining the above mentioned techniques, the overall PDP value can be reduced up to 23%, as Fig. 4(d) shown. By connecting two PMOS diodes, the conventional cross-coupled level converter can successfully convert the signal from the sub-threshold region to super-threshold region. Using multi-V_{th} devices improve the performance and the leakage reduction technique compensates the LTV logic leakage problem. The reverse short channel effect and inner inverter device sizing make the proposed level converter more robust and reliable.

G. *A dual edged-triggered explicit-pulsed level-converting flip flop combining a modified DCVSPG latch concept*

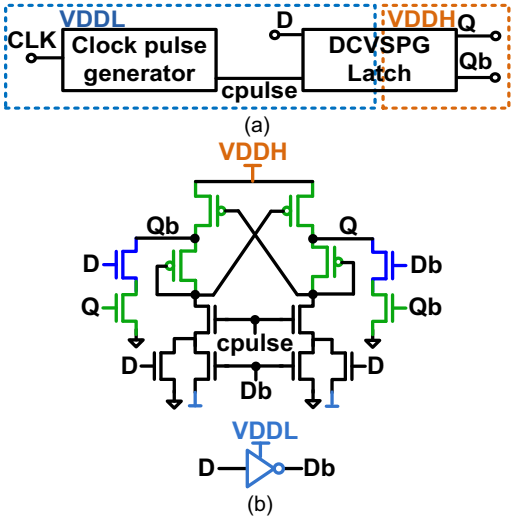


Figure 6: (a) The proposed dual edge-triggered explicit-pulsed level-converting flip flop. (b) A modified DCVSPG latch

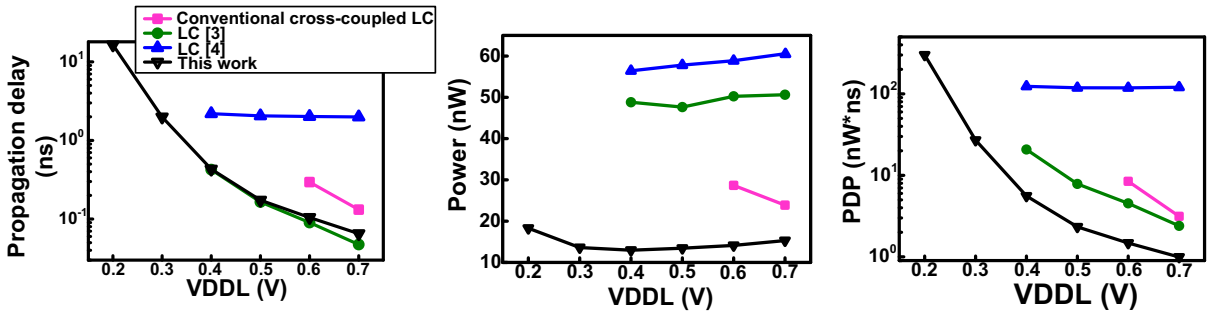
A traditional dual edge-triggered explicit-pulsed level-converting flip flop (LCFF) consists of a clock pulse generator and a latch, as shown in Fig. 6(a). The clock signal and data input with a low supply voltage are leveled up to produce a high voltage stored output. However, as the input signal voltage scales down to the sub-threshold region, the traditional LCFF encounters an imbalance driving ability so that fails to function correctly. The original DCVSPG was first presented in [12]. In order to address the imbalance difficulty, a modified DCVSPG latch with our level converter concept is proposed. With the effective techniques presented in this section, the modified DCVSPG latch can function correctly even when supply voltage is down to sub-threshold region, as shown in Fig. 6(b).

III. SIMULATION RESULTS

For comparison, we implemented the following three level converters: conventional cross-coupled type, short current reduction type in [3] and two cross-coupled cascaded type in [4]. Iso-area analysis is used for the fair comparison.

A. *Minimum input voltage*

Comparing with the other three level converters, the proposed level converter has a minimum input voltage below the target voltage 200mV, as Fig. 7 shown. The minimum input voltage is defined as an input voltage which the level converter can function correctly at five process corners. We set VDDH to 1.0V at room



(a) (b) (c)

Figure 8: Performance comparison between the proposed level converter and the existing level converter: (a) propagation delay comparison (b) power comparison (c) PDP comparison

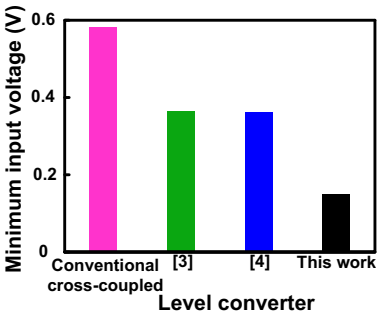


Figure 7: Minimum input voltage comparison

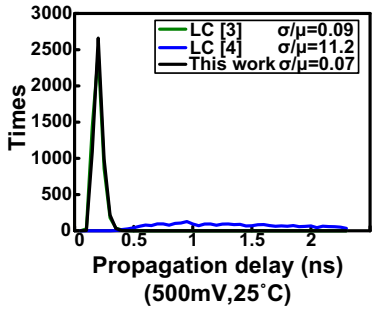


Figure 9: Monte Carlo simulation for propagation delay when supply voltage is 500mV

temperature and swept the input voltage from 100mV to 1.0V at five process corners. For the sub-threshold level converter, the NMOS transistor should overpower the corresponding PMOS transistor to make the switch successfully. Therefore, the worst case is slow NMOS-slow PMOS corner. The minimum input voltage of the worst case is 150mV. Typical NMOS-typical PMOS and fast NMOS-fast PMOS are the best cases. The minimum input voltage of the best case is as low as 100mV. From the simulation, the proposed level converter has a wide operation range.

B. Propagation delay, Power, and PDP

The propagation delay comparison is drawn in Fig. 8(a). Our work is slight slower than the level converter in [3] when supply voltage is higher than 0.5V. The level converter in [4] provides a slow speed because of a cascaded architecture. For the propagation delay comparison, the proposed level converter shows a better performance when operated in the sub-threshold region. The power consumption comparison is shown in Fig. 8(b). Due to the leakage reduction technique, the LTV device leakage problem is compensated. Also, the reverse short channel effect device sizing helps the proposed level converter consumes less power. PDP comparison is drawn in Fig. 8(c). Our work presents a small PDP value, especially when operating at higher supply voltage. The proposed level converter is more energy-efficient.

C. Monte Carlo simulation

Fig. 9 presents 5000-point Monte Carlo simulations for the supply voltage 500mV. Monte Carlo simulation demonstrates how the process variations affect the level converter characteristics. For the near-threshold region, the proposed level converter has the normalized variance value σ/μ is 0.07, which is a relatively small value among the other two level converter. Our work shows the less sensitivity towards the process variations. The proposed level converter is more robustness than the other two level converters in [3] and in [4].

D. Temperature-induced delay variation

MOSFET mobility and threshold voltage are changed with the temperature. Consequently, the drain current is related with the temperature. We swept the temperature from 0˚C to 125˚C and measured the temperature variations on the propagation delay. For the simplicity, take the absolute value of the propagation delay difference as the temperature-induced variation delay.

Table 1.Performance Summary and Comparisons

	[2]	[3]	[4]	This work
Technology	0.18μm	0.18μm	130nm	65nm
Propagation Delay	10μs@127mV	6.3ns@400mV	35ns@227mV	52ns@150mV
Power Consumption	20μW	7.9μW	N.A.	21nW
VDDH	1.8V	1.8V	1.2V	1.0V
Minimum Input Voltage	127mV	400mV	227mV	150mV
Transistor Numbers	10	14	11	12

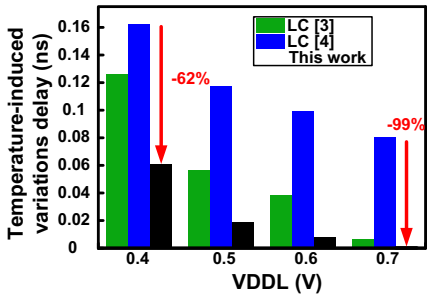


Figure 10: Temperature-induced variations on propagation delay

Comparing with the other two level converters in [3] and [4], Fig. 10 presents that the proposed level converter has less the temperature effects on the propagation delay. The temperature variations on the delay can be reduced up to 99% at the higher supply voltage. Thus, the proposed level converter is more process, voltage, temperature robustness.

IV. CONCLUSIONS

A power-delay-product optimized and robust level converter is presented for sub-threshold to super-threshold signal converting. By combining energy-efficient techniques, PDP value of this work is decreased by 23%. Temperature induced variation on propagation delay is reduced up to 99%. The performance summary of the proposed level converter is given in Table. 1. The performance comparisons with [2]-[4] are also listed. This work provides a wide operation range, from 150mV to 1V across five process corners under TSMC 65nm bulk CMOS technology. When the input voltage is 150mV, it can achieve a propagation delay of 52ns and consume only 21nW. The proposed level converter can be applied to a dual edged-trigged explicit-pulsed level-converting flip flop with a modified DCVSPG latch. It is suitable to be the interface of two different voltage domains in emerging dynamic voltage frequency scaling wireless applications.

REFERENCES

1. J.-C. Chi, H.-H. Lee, S.-H. Tsai, and M.-C. Chi, “Gate Level Multiple Supply Voltage Assignment Algorithm for Power Optimization Under Timing Constraint” *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 15, No. 6, pp. 637-648, Jun. 2007.
2. H. Shao and C.-Y. Tsui, “A Robust, Input Voltage Adaptive and Low Energy Consumption Level Converter for Sub-threshold Logic,” *European Solid State Circuits Conference,* pp.312-315, Sept. 2007.
3. S. Ali, S. Tanner, and P.A. Farine, “A Robust, Low Power, High Speed Voltage Level Shifter with Built-in Short Circuit Current Reduction,” *IEEE European Conference on Circuit Theory and Design*, pp. 142-145, Aug. 2004.
4. S. N. Wooters, B. H. Calhoun, and T. N. Blalock, “An Energy-Efficient Subthreshold Level Converter in 130-nm CMOS,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol.57, No. 4, pp. 290-294, Apr. 2010.
5. S. Lütkemeier and U. Rückert, “A Subthreshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror,” *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 57, No. 9, pp. 721-724, Sept. 2010.
6. A. Hasanbegovic and S. Aunnet, “Low-Power Subthreshold to Above Threshold Level Shifter in 90 nm Process,” *NORCHIP,* pp. 1-4, Nov. 2009
7. I.-J. Chang; J.-J. Kim; K. Kim, and K. Roy, “Robust Level Converter for Sub-Threshold/Super-Threshold Operation: 100 mV to 2.5 V,” *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 19, No. 8, pp.1429-1437, Aug. 2011.
8. Y.-S. Lin and D. Sylvester, “Single Stage Static Level Shifter Design for Subthreshold to I/O Voltage Conversion,” *IEEE International Symposium on Low Power Electronics and Design*, pp. 197-200, Aug. 2008.
9. Y. Chavan and E. MacDonald, “Ultra Low Voltage Level Shifter to Interface Sub and Super Threshold Reconfigurable Logic Cells,” *IEEE Aerospace Conference*, pp. 1-6, Mar. 2008.
10. K.-H. Koo, J.-H. Seo, M.-L. Ko, and J.-W. Kim, “A New Level-Up Shifter for High Speed and Wide Range Interface in Ultra Deep Sub-Micron,” *IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 1063-1065, May 2005.
11. K. Agarwal, V. Venkateswarlu, and D. Anvekar, “A Level Shifter Deep-Submicron node using Multi-Threshold Technique,” *IEEE Recent Advances in Intelligent Computational Systems,* pp. 925-929, Sept. 2011.
12. F.-S. Lai and W. Hwang, “Design and implementation of differential cascode voltage switch with pass-gate (DCVSPG) logic for high-performance digital systems,” *IEEE Journal of Solid-State Circuits,* Vol. 32, No. 4, pp. 563-573, Apr. 1997.