An All-Digital Read Stability and Write Margin Characterization Scheme for CMOS 6T SRAM Array

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***Abstract*—We present an all-digital Read Stability and Write Margin (WM) characterization scheme for CMOS 6T SRAM array. The scheme measures the cell Read Disturb voltage (V_{read}) and cell Inverter Trip voltage (V_{trip}) in SRAM cell array environment. Measured voltages are converted to frequency with Voltage Controlled Oscillator (VCO) and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. Resistor based voltage divider with 64 voltage levels and 10mV per step is employed to allow sweeping of BL voltage from 640mV to GND for WM characterization. A 512Kb test macro is implemented in UMC 55nm 1P10M Standard Performance (SP) CMOS technology. Monte Carlo simulations validate the accuracy of V_{read} and V_{trip} measurement scheme, and post-layout simulations show the resolution of the digital read-out scheme is 0.167mV/bit.**

I. Introduction

The cell stability, Static Noise Margin (SNM) [1], and V_{MIN} of CMOS 6T SRAM are limited by leakage, variation, and supply voltage in the physical domain [2-7], and conflicting Read/Write requirements and cell disturb in the design domain. With technology scaling, the variations in cell Read-Disturb voltage (V_{read}) (Fig. 1) and cell Inverter Trip voltage (V_{trip}) increase, causing overlap and Read failure [8]. Various measurement techniques have been developed to characterize SRAM bit cell transistors, Read Stability and Write Margin (WM) [9]. While individual cell/device based characterization structures [10] can offer detail characteristics of the individual subjects, it is preferable and essential to characterize the Read Stability and WM in product array like environment so as to capture all the lithography and process related effects [11-14]. It is also important that the layout surrounding measured devices is as close as possible to the layout of the original SRAM array to incorporate the effects of dense layout and the applied ground rule waivers not present in isolated single transistor or cell.

In this work, we present an all-digital Read Stability and Write Margin (WM) characterization scheme for CMOS 6T SRAM array. The scheme measures the cell Read Disturb voltage (V_{read}) and cell Inverter Trip voltage (V_{trip}) in SRAM cell array environment. Measured voltages are converted to frequency with Voltage Controlled Oscillator (VCO) and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. Resistor based voltage divider with 64 voltage levels is employed to allow sweeping of BL voltage for WM characterization. Section II describes the modified cell structure, measurement scheme and Monte Carlo simulation results to validate the measurement scheme. Section III presents the test macro architecture and digital read-out scheme. Section IV discusses the 512Kb test macro implementation in UMC 55nm CMOS technology. The conclusions of the paper are given in Section V.

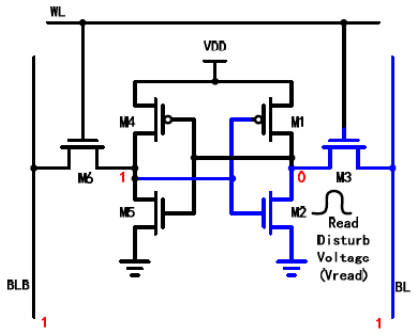

Fig. 1. Standard 6T SRAM cell in Read mode.

II. Measurement Schemes for V_{READ}, V_{TRIP} and WM

A. Modified Cells for V_{read} and V_{trip}

Fig. 2 and Fig. 3 depict the schematic, modification of the cell layout and the equivalent circuit for V_{read} and V_{trip} measurement, respectively. For 6T SRAM, thin cell layout with horizontal uni-directional poly, and pattern density/symmetry are crucial for manufacturability and yield, especially for poly, diffusion and contact layers. To blank out unused cell devices and alter connections while preserving the layout and surroundings of critical layers, we keep the diffusion, poly and contact layers intact, and only modify Via and metal layers as shown in Fig. 2(b) and 3(b).

To measure V_{read}, the left cell inverter is blanked out with its supply and GND nodes left floating. The input of the right cell inverter (gate of M1/M2) is connected to V_{DD} to force the right cell storage node Q to "Low", corresponding to the condition for Read operation. The column structure for V_{read} measurement is shown in Fig. 4(a). In V_{read} measurement mode, "V_{read_enb}" goes "Low", and the Read conditioning PMOS precharges and holds BL at V_{DD}. The voltage at node Q, resulting from the voltage divider effect from right access transistor M3 and right pull-down NMOS M2, will be V_{read}, and is passed through the left access transistor M6 to BLB for measurement.

For V_{trip} measurement , the left cell inverter is blanked out with its supply and GND nodes left floating. In V_{trip} measurement mode, "V_{trip_enb}" (Fig. 4(b)) goes "Low", The Trip conditioning PMOS equalizes (i.e. shorts) the voltages of BL and BLB, which in term forces the input and output of the right cell inverter (M1/M2 in Fig. 3) to equal potential at V_{trip}.

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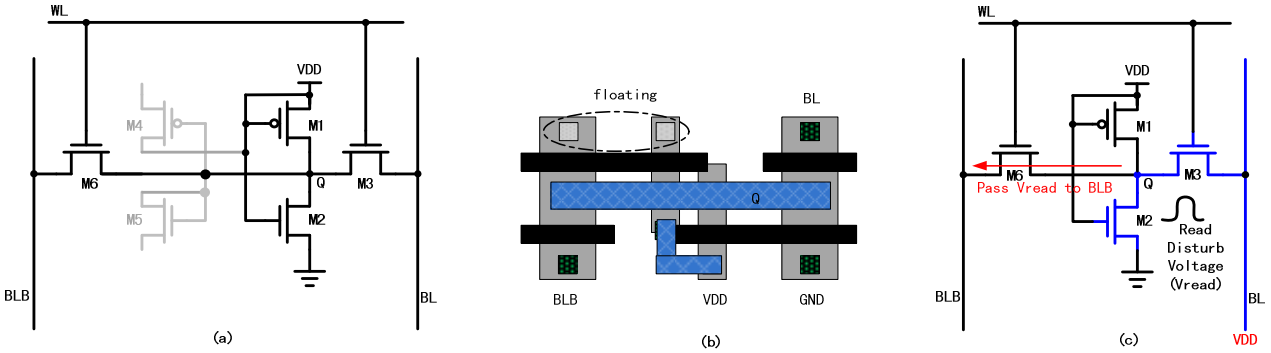


Fig. 2. (a) V_{read} cell schematic, (b) V_{read} cell layout and (c) V_{read} cell equivalent circuit.

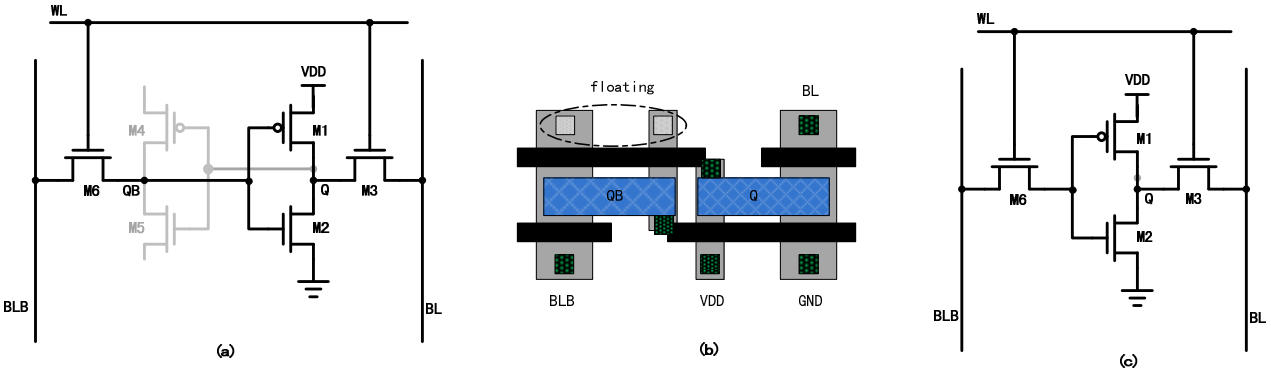


Fig. 3. (a) V_{trip} cell schematic, (b) V_{trip} cell layout and (c) V_{trip} cell equivalent circuit.

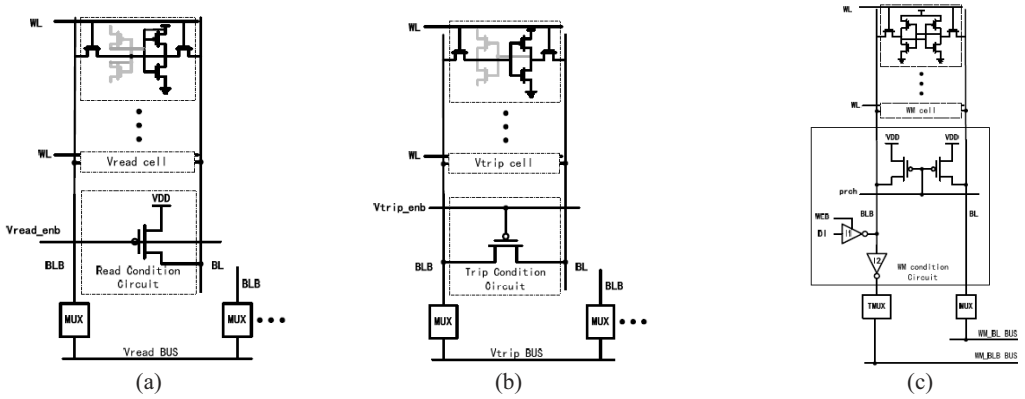


Fig. 4. Column structure for (a) V_{read} , (b) V_{trip} and (c) WM measurement.

Fig. 5 compares the Monte Carlo simulation results (290000 samples) of V_{read} and V_{trip} distributions of the proposed scheme with that of a single isolated cell inverter. The distribution of the proposed scheme can be seen to track that from single isolated cell inverter very well.

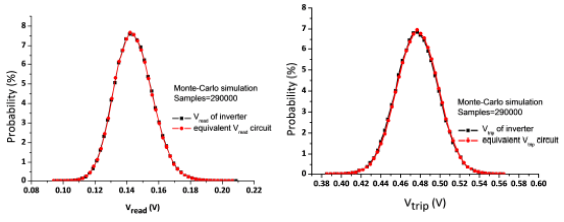


Fig. 5. Comparison of Monte Carlo simulation results for (a) V_{read} and (b) V_{trip} of proposed scheme with that of isolated cell inverter.

B. Write Margin (WM) measurement

Resistor based voltage divider with 64 voltage levels and 10mV per step is employed to allow sweeping of BL voltage from 640mV to GND for WM characterization. In WM measurement mode, background data of "1" (Q = 1) are written into the cell array. Then, "WEB (Write Enable BAR)" (Fig. 4(c)) goes "Low", enabling gated inverter I1 to clamp BLB at V_{DD}. The output from the resistor based voltage divider is fed into BL through an unity gain buffer to "Write" the selected cell to "0". "WEB" then goes "High" to disable gated inverter I1, and the data in the selected cell is sensed (i.e. Read) by sensing inverter I2 from BLB to decide whether the Write operation has been successfully performed.

III. Test Chip Architecture and Digital Read-out Scheme

Fig. 6 shows the measurement array architecture. To reduce pin count for the control signals and input address, shift registers are employed for both row and column decoders. The columns for V_{read}, V_{trip}, and WM measurement are interleaved with independent set of column shift registers. For WM measurement, it is necessary to stay at the same selected WL through Write (WM Measurement)-Read (Verify whether Write is successful)-Write (Write original data back into selected cells) sequence while sweeping through the BL voltage step. Two types of shift registers are employed: the column shift register (Fig. 7(a)) for normal sequential shift and the row shift register (Fig. 7(b)) with the added capability of holding the previous data (for staying at the same WL for WM measurement). To prevent the voltage level degradation through the column mux, full transmission gate with high gate control voltage of 1.2V is use. The rest of the design including supply for cell array operates at 1.0V.

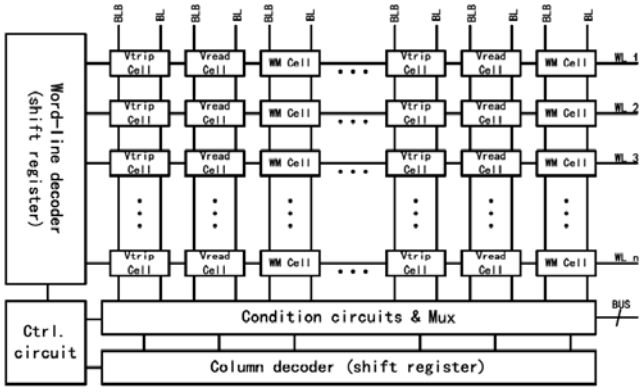
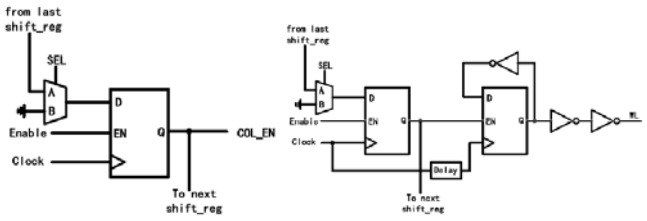


Fig. 6. Measurement Array Architecture.



(a) (b)

Fig. 7. (a) Column shift register and (b) row shift register.

The bit-line length is 128 cells. Each bank comprises 128 WL and 85 sets of interleaved V_{read}, V_{trip} and WM columns (a total of 3x85 columns). So there are about 128x85x3~32K cells in a bank. With 16 banks, the total cell number is 16x32K ~ 512Kb. For each V_{read}, V_{trip} or WM measurement, we can obtain 128x85x16=174.08K samples.

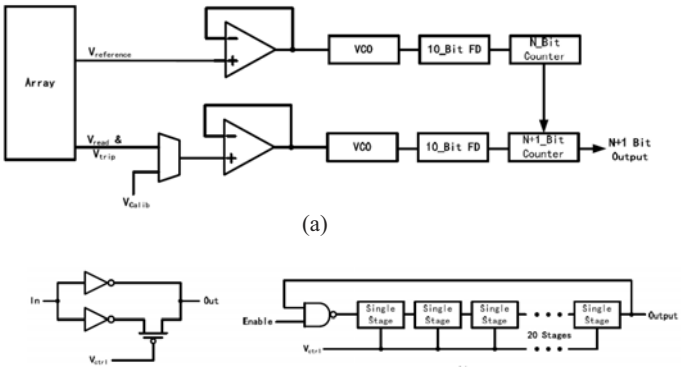


Fig. 8. (a) VCO and counter based digital read-out scheme and (b) single stage (left) of 21 stage VCO (right) [15].

To facilitate extraction, processing, and statistical analysis of large amount of data, a VCO (Voltage Controlled Oscillator) and counter based digital read-out scheme (Fig. 8 and 9) similar to that in [15] is employed. The measured analog voltage is fed into an unity-gain buffer, converted into frequency by VCO, divided through a 10-bit Frequency Divider (FD) and read-out by the counter. Reference and calibration paths are provided. Since the voltage levels of measured V_{read} and V_{trip} are low (< 1/2 V_{DD}), P-type VCO with PMOS delay control device (Fig. 8(b)) is employed so the measured analog voltage (the control voltage at the gate of PMOS delay control device) is at where the VCO sensitivity is maximum. This provides a sensitivity of about 480MHz/V (Fig. 10) for the VCO. The resolution of the counter depends on number of bits and the period of counting. The 13-bit counter in the Reference path is used to set the counting period of the 14-bit counter in the measurement path which does the actual counting. This provides a resolution of about 0.167mV/bit.

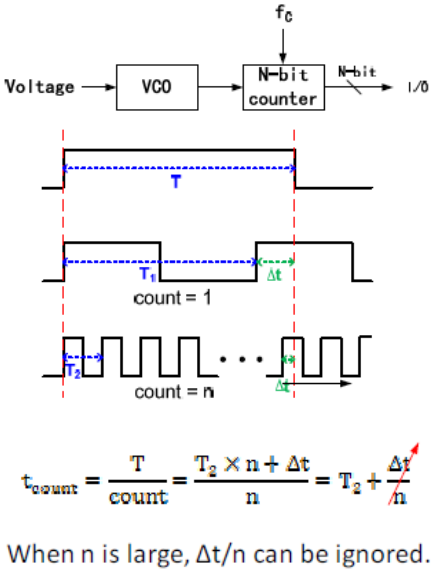


Fig. 9. Counting period and VCO resolution.

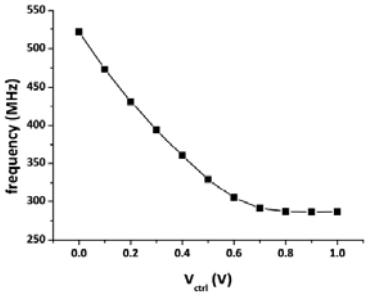
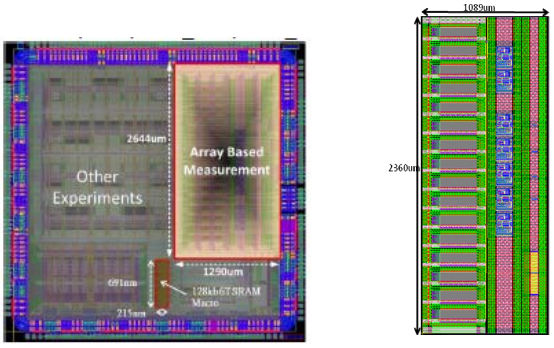


Fig. 10. Sensitivity of P-type VCO in Fig. 8(b).

IV. Test Macro Implementation

The 512Kb test macro is implemented in UMC 55nm 1P10M Standard Performance (SP) CMOS technology. This array based measurement macro is located at the upper right corner of the test chip (Fig. 11(a)). The layout view of the test macro is shown in Fig. 11(b)). The test array has two power domains: 1.2V for the full transmission gate column mux, and 1.0V for the cell array and other peripheral circuits. The total number of OP-Amp is 7 (2 for V_{read} measurement, 2 for V_{trip} measurement, 1 for resistor based voltage divider output for WM measurement, and 2 for calibration) . All OP-Amps are located at the middle strip of the macro with a 3.3V supply. Four VCO's and resistor voltage divider are located at the right side of the macro with their own supply. The overall macro area is 2644 μ mx1290 μ m (excluding FD and counter) with 27 pins. The characteristics of the test macro are summarized in Table-I.



(a) (b)

Fig. 11. (a) Array based measurement macro (upper right) in test chip and (b) layout view of array based measurement macro.

V. Conclusions

We presented an all-digital Read Stability and Write Margin (WM) characterization scheme for CMOS 6T SRAM array. The scheme measured the cell Read Disturb voltage (V_{read}) and cell Inverter Trip voltage (V_{trip}) in SRAM cell array environment. Measured voltages were converted to frequency with Voltage Controlled Oscillator (VCO) and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. A 512Kb test macro was implemented in UMC 55nm CMOS technology. Post-layout simulations showed the resolution of the digital read-out scheme is 0.167mV/bit.

Table-I : 512Kb Test Macro Characteristics

Capacity	Total 512 K bits
Process	55nm 1P10M SPRVT + HVT_6TSRAM
Area	
32 K-bit bank	445.9 um × 150.7 um
OP	143.2 um × 170.9 um
VCO	50.4 um × 4.83 um
Overall	1290 um × 2644um (excluding FD and counter)
Gain of VCO	482.2 MHz/V (@V_c=0V) 243.3 MHz/V (@V_c=0.6V)
Resolution of Counter based measurement circuit	0.167 mV

Acknowledgment

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