An Efficient Power Management System for Solar Energy Harvesting Applications

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Abstract — An efficient power management system for solar energy harvesting applications is proposed. The system accepts energy from PV cell or battery and outputs 500mV, 1V and -500mV to load circuitry. When solar energy is available, the system is powered by photovoltaic (PV) cell. On the other hand, the battery will supply energy to the system when there is no solar energy. With proposed control unit, the energy consumption of battery decreased 80%. The maximum total power efficiency is 69%. All results are simulated in UMC 90nm CMOS technology model.

Index Terms — Power management, solar energy, regulator, clock generator.

I. INTRODUCTION

Recently the market of portable devices is growing rapidly. Low power consumption is the top requirement. And due to energy crisis and eco-awareness, the usage of environmental energy harvesting, such as solar and wind energy, also gains more attention. Maximum output power tracking system of photovoltaic cell was implemented [1]. Ultra-low voltage power management for energy harvesting applications was developed and worked with a FIR filter [2]. Micro power management system was presented [3] to cope with low output voltage of solar cell. The micro power management system decided the working frequency of charge pump according to room lighting environment and output the maximum power to load circuitry. An energy harvesting application with micro battery was also implemented [4] to accept energy from RF and thermal power and output the power to micro battery as energy storage. A battery management system for solar energy applications was developed [5]. The battery management system was used to increase the service life of the battery.

In this work, we develop an efficient power management system that is powered by solar energy and outputs three different voltage level for computation circuitry or memory circuitry. We also proposed a control unit circuit within the power management system to reduce energy waste of battery when the system is powered by rechargeable battery. A power efficiency optimization unit is designed for 1V generator. In light loading case, the power efficiency optimization unit outputs low frequency clock to charge pump. This will reduce the power consumption. In heavy loading case, the frequency of clock is increased for keeping the output voltage level of 1V generator. The detail circuitry is described in Section II. Section III shows the simulation results and Section IV concludes this paper.

II. POWER MANAGEMENT SYSTEM

The architecture of the proposed power management system is shown in Fig. 1. It contains a PV cell, a control unit, a voltage regulator, a clock generator, a voltage generator, a battery charger and a rechargeable battery.

The voltage regulator provides a basic 500mV operating voltage to clock generator, voltage generator, battery charger and power efficiency optimization unit. It also supplies 0.5V to computation circuitry. The voltage generator and battery charger is composed of charge pump. The 1V generator can supply 1V to circuits which require higher voltage while the -0.5V generator supplies -0.5V to whom requires negative voltage. The power efficiency optimization unit supplies a variable frequency clock to 1V generator. The PV cell and battery are also implemented in circuit model and simulated with power management system.

A. Photovoltaic (PV) Cell

The I-V curve and P-V curve of PV cell is shown in Fig. 2. The black line is the I-V curve of output load.
current versus output voltage of PV cell. The output voltage of PV cell is between 0mV and 840mV. The red line shows the P-V curve of the output power versus the output voltage of PV cell. The maximum output power of PV cell is 2.3mW.

B. Control Unit (CU)

Due to two different supply voltage sources of power management, we design a control unit to increase power efficiency of the overall system. The block diagram of control unit is shown in Fig. 3.

When the PV cell supplies energy to voltage regulator, the voltage of node 1 is higher than node 2. The direction of current flow is from node 1 to node 2. The OP amplifier will output “1” to inverter and MP1 will be turned on. In this case, the battery charger is active. When the battery supplies energy to voltage regulator, MP1 will be turned off to decrease the current flow back to PV cell. The battery charger will also be disabled. The energy consumption of battery is decreased by 80%.

C. Voltage Regulator

The voltage regulator is composed of a differential amplifier, an inverter as a buffer and a power PMOS. The schematics of voltage regulator are shown in Fig. 4. As voltage of Vregu drops down, the MP_{AUX} will supply more current to differential amplifier. Thus, the MP_{OUT} will turn on rapidly and supply more current to Vregu node. When there is no load current, MP_{AUX} will slightly turn on and decrease the power consumption of differential amplifier.

D. 1V and -0.5V Voltage Generators

The 1V and -0.5V are generated by charge pumps. The circuit of 1V generator and -0.5V generator is shown in Fig. 6. The CCLK, CCLKB, NCLK and NCLKB are supplied by voltage regulator, which is 0.5V. The CCLK, CCLKB, NCLK and NCLKB are constant frequency clock. The 1V generator is a voltage doubler. It accepts the supply voltage of 0.5V from voltage regulator and output 1V to load circuitry. The CLK and CLKB are from power efficiency optimization unit. The negative voltage generator takes GND as input voltage. With NCLK and NCLKB switching, the output voltage will be pumped down to -0.5V.

E. Battery Charger

The schematic of battery charger is shown in Fig. 6. In this work, the clock signal is supplied by voltage regulator, which is 0.5V. The initial state is that node 1 = 0V and node 2 = 0V. When CLK=0.5V, the node 1 is 0.5V and node 2 is “0.5V-Vtn”. When CLKB=0.5V, the node 2 is “1V-Vtn” and the node 1 is 0.5V. As the node CLK is charge to 0.5V again, the node 1 is 1V. In first stage, the node 1 and node 2 will vibrate between 0.5V and 1V. The NMOS capacitors of second stage are connected to node 1 and node 2. Thus the node 3 and node 4 will vibrate between 1V and 1.5V. After multiple stages, the node OUT will be 2.5V.
F. Clock Generator

The clock system consists of two parts. The constant clock generator is used to serve the battery charger and the -0.5V generator. The variable clock generator is designed to serve 1V generator. It is controlled by the power efficiency optimization unit.

The schematic of proposed variable clock generator is shown in Fig. 8. It contains a basic ring oscillator and two transmission gates between the inverters. The frequency of variable clock is controlled by the voltage bias of Vp and Vn. When Vp goes down and Vn goes high, the delay time of transmission gate is reduced as well as the frequency of the clock rise, and vice versa. Vp and Vn is biased by the net bias circuit. The variable clock generator achieves wide frequency range and low power. It can provide frequency range from 33MHz to 300MHz. the power consumption is 29uW when operated at 300MHz including the net bias circuit.

G. Power Efficiency Optimization Unit

The power efficiency optimization unit controls the clock frequency of variable clock generator and optimizes the power efficiency of 1V generator according to the loading condition. The power efficiency unit used voltage detector to detect the loading condition of the 1V generator output. The proposed voltage detector is shown in Fig. 8. When the output voltage of 1V generator decrease, vd will increase and it will be compare to the vref. The detecting flag will be sent according to the result of comparison.

If the load current increase and output voltage of 1V generator is below 900mV, the flag will disable and the clock frequency of variable clock generator will decrease until reach the minimum clock frequency.

The power efficiency of proposed optimization unit compare to supply with constant clock is shown in Fig. 9. With the dynamic detection, the system achieves better power efficiency compared to supply with constant clock under different load current condition.

III. SIMULATION RESULTS

The design is implemented in UMC 90nm CMOS technology. The layout view of the power management system is shown in Fig. 10.

A. PV Variation

The supply current of PV cell varies from 4mA to 0mA. The different output voltages are shown in Fig. 11. The PV cell outputs zero current at 10us to demonstrate the function of control unit. The first row is output voltage of PV cell which varies from 840mV to 177mV. The second row is output voltage of voltage regulator. It varies from 592mV to 482mV. The third row is 1V generator, ranging from 1.11V to 0.9V. The fourth row is -0.5V generator. It varies from -547mV to -440mV.
The difference of power management system with and without CU is shown in Fig. 12. The PV cell is set to output zero current and the power management system is supplied by battery.

Without control unit, the PV cell is connected directly to voltage regulator, the output current of battery is 961μA in 30ns. With the control unit, the output current of battery is reduced to 200μA in 30ns.

The simulation result shows that with CU, the power consumption of battery will be reduced 80% compare to power management system without CU. This will increase the usage time of battery. The specifications of power management system are summarized in Table I. All results are simulated in typical case.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>POWER MANAGEMENT SYSTEM FOR SOLAR ENERGY HARVESTING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>UMC 90nm CMOS Technology</td>
</tr>
<tr>
<td>Output current of PV cell</td>
<td>4mA–0</td>
</tr>
<tr>
<td>Output voltage of PV cell</td>
<td>840mV–177mV</td>
</tr>
<tr>
<td>Output power of PV cell</td>
<td>2.3mW–0mW</td>
</tr>
<tr>
<td>0.5V output</td>
<td>592mV–482mV</td>
</tr>
<tr>
<td>1V output</td>
<td>1.11V–0.9V</td>
</tr>
<tr>
<td>-0.5V output</td>
<td>-547mV–-440mV</td>
</tr>
<tr>
<td>Maximum total power efficiency</td>
<td>69%</td>
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</tbody>
</table>

III. CONCLUSIONS

An efficient power management system is proposed. The power management system works with PV cell and rechargeable battery. The output current of PV cell varies from 0 to 4mA and its output voltage varies from 177mV to 840mV. The power management system outputs voltage of 0.5V, 1V and -0.5V to loading circuitry. The 0.5V output varies from 482mV to 592mV. The 1V output varies from 0.9V to 1.11V. The range of -0.5V output is -440mV to -547mV. With control unit and power efficiency optimization unit, the battery supplies energy efficiently and the power consumption is down to one fifth (20%). The maximum total power efficiency is 69%.

REFERENCES