Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array

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***Abstract*—One of the major reliability concerns in nano-scale CMOS VLSI design is the time-dependent Bias Temperature Instability (BTI) degradation. Negative Bias Temperature Instability and Positive Bias Temperature Instability (NBTI and PBTI) weaken MOSFETs over usage/stress time. We present an embedded 6T SRAM ring oscillator structure which provides in-situ measurement/characterization capability of cell transistor degradation induced by bias temperature instability. The viability of the embedded ring oscillator odometer and the impact of bias temperature instability are demonstrated in 55nm standard performance CMOS technology.**

I. INTRODUCTION

Lifetime reliability is one of the key design factors for robust VLSI systems. Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB) have become major concerns for performance and yield of nano-scale CMOS VLSI systems. These reliability degradations not only constrain the technology scaling, but also threaten the stability and functionality of digital circuits [1-4]. The degradation of device threshold voltage under the presence of electrical and thermal stress has long been a significant reliability issue in scaled CMOS technologies. Due to the importance of long-term degradation in nano-scale CMOS SRAM, there have been significant amount of efforts investigating the impacts of NBTI and PBTI on SRAM static/dynamic noise margins and cell failure probability [1, 2]. Kang et al. [2] explored the impact of NBTI degradation of several critical performance parameters of SRAM arrays. They showed that, under NBTI stress, the Static Noise Margin (SNM), READ stability, and parametric yield of SRAM array were severely degraded over time. On the other hand, Write-ability and leakage current might improve with time. Bansal et al. [3] carried out failure analysis using Monte-Carlo simulations and showed that, under worst-case static stress, NBTI and PBTI degraded the stability during READ (significantly) and WRITE (marginally) operations.

Ring Oscillator (RO) based structure for measuring NBTI degradation is the simplest method [5]. It has been shown that the relative degradation of NBTI stressed ring oscillator increases as the operating voltage decreases. Some on-chip reliability monitors for measuring degradation of digital circuits have been proposed [5-7].The circuits in [5] overcome the drawbacks of conventional ring oscillators which fail to isolate the NBTI and PBTI contribution when PBTI isn't negligible anymore in deeply-scaled CMOS technology with high-κ/metal-gate [8, 9]. Kim et al. [6] developed a silicon odometer with high sensing resolution by measuring the beat frequency of two ring oscillators. Furthermore, a monitoring structure [7], which can measure the frequency degradation induced by HCI, BTI, and TDDB separately, has been introduced for accurate real-time reliability monitoring. However, all of these monitoring structures were implemented in logic circuits with individual isolated logic devices to characterize the BTI effects on general digital logic devices/circuits, not for specific SRAM cell transistors in a real SRAM cell array environment.

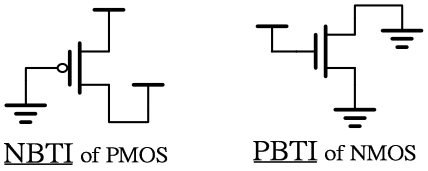

Fig. 1. NBTI stress of PMOS and PBTI stress of NMOS.

In this work, we propose an embedded SRAM ring oscillator structure and measurement technique to characterize the BTI degradation of 6T SRAM cell transistors in a real SRAM cell array environment. The embedded ring oscillators are built using the 6T SRAM cell transistors directly in a real SRAM cell array environment, thus providing direct correlation between measured BTI degradation of cell transistors and the resulting impacts on SRAM stability. The details of the Embedded SRAM Ring Oscillator (ESRO) are presented in Section II. The analysis and measurement results are shown in Section III, and the conclusions of the paper are given in Section IV.

II. EMBEDDED SRAM RING OSCILLATOR

A. Embedded SRAM Ring Oscillator and BTI Stress

Fig. 1 shows a PMOS (NMOS) under NBTI (PBTI) stress, As mentioned above, the SRAM stability degradation induced by BTI significantly impacts the long-term reliability. As such, it is crucial to have a characterization structure that can provide direct measurement of cell transistor degradation due to aging effects. We modify the SRAM cell array to form an ESRO for BTI measurement. We combine the BTI stress capability and ring oscillator into ESRO structure. In 6T SRAM cell (Fig. 2), we are mainly concerned about the degradation of pull-up PMOS (NBTI) and pull-down NMOS (PBTI). The degradation of these two devices can affect the cell stability and performance significantly. For the access pass-gate transistor, the active period for a particular WL is typically relatively short during the whole SRAM operation.

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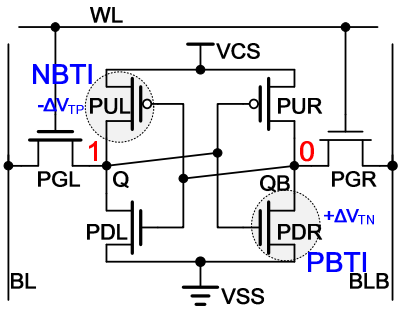

Fig. 2. A 6T cell suffers asymmetrical degradation from NBTI and PBTI.

Therefore, compared with pull-up PMOS and pull-down NMOS, the stress period of pass-gate transistor is much shorter, and the BTI induced threshold voltage degradation of pass-gate transistor is negligible.

Fig. 3 shows an inverter stage in a ring oscillator, If the input of inverter is '0', the PMOS is under NBTI stress while the NMOS is not stressed. Meanwhile, the supply voltage can be raised to Vstr to enhance the stress efficiency. On the other hand, when the input is '1', the NMOS is under PBTI stress, and higher Vstr at the input can speed up the NMOS degradation.

B. Embedded 6T SRAM Ring Oscillator Structure

The unit-stage of ESRO, as shown in Fig. 4(a), is composed of two parts/cells: blanked-cell (for control and stress) and active-cell (for forming an inverter). The major function of blanked-cell is to provide the stress voltage to the input of active-cell inverter for stressing PMOS or NMOS, and we use PMOS (P_SWITCH) in the blanked-cell as a switch. During Stress NMOS mode, $CTRL_{STR}$ is pull down to '0' to turn on P_SWITCH for passing V_{B_STR} to the input of active-cell inverter. With a "High" at active-cell inverter input, the NMOS is under PBTI stress. Complementarily, we provide a '0' signal at the input of active-cell inverter for NBTI stress of PMOS. Due to the poor ability of PMOS to pass '0', we pull down $CTRL_{STR}$ to a negative voltage to over-drive P_SWITCH to pass a stronger '0' to the input of the active half-cell inverter. The supply voltage of the active-cell can be pulled up to a higher voltage to enhance NBTI stress of PMOS.

The Device Under Test (DUT) is the pull-up PMOS (PU_INV) and the pull-down NMOS (PD_INV) in the active-cell. The pass-gate in the active-cell controls the connection of the ring oscillator. During Stress mode, the unit-stage inverter is isolated from the previous and succeeding inverters by the pass-gates in the active-cells (The Word-Line (WL) is "0" to turn off the pass-gate transistors). The other devices in the cell are blanked out to break the feedback loop so as not to affect the normal ring oscillator operation. The blanked-cells and active-cells use two independent power supply lines, V_{B_STR} and V_{A_STR}. Both of them can be set up at different levels under different operation modes. The overall input conditions for Stress Mode and Measurement Mode are shown in Table 1.

For a 6T SRAM, thin cell layout with horizontal uni-directional poly, and pattern density/symmetry are crucial for manufacturability, especially for the poly, diffusion and contact layers. To blank out unused cell devices, we keep the

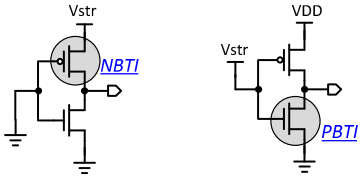

Fig. 3. One stage inverter under stress of NBTI and PBTI.

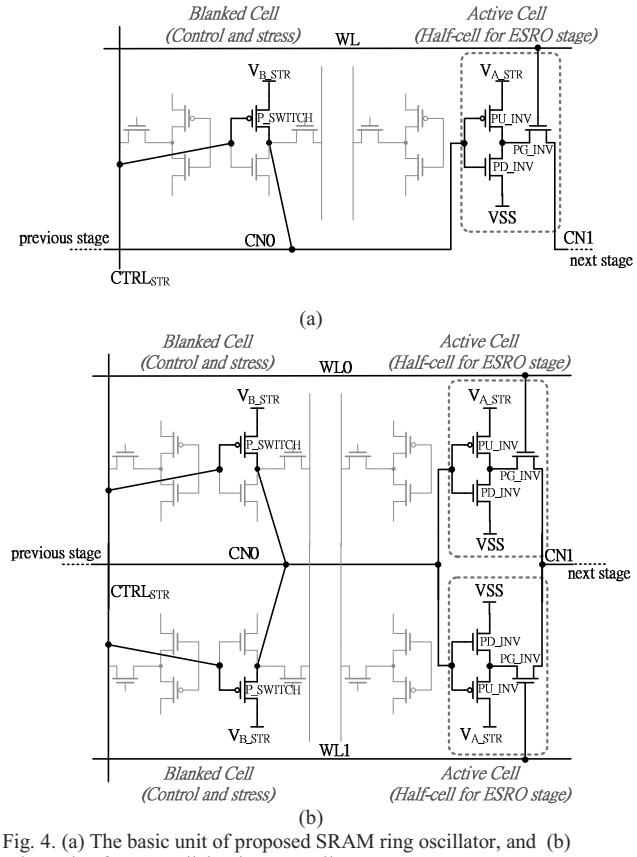

Fig. 4. (a) The basic unit of proposed SRAM ring oscillator, and (b) schematic of two parallel unit-stage cells.

Table 1. Input Conditions for Embedded SRAM Ring Oscillator

Signal	Stress Mode		Meas. Mode
	NBTI	PBTI	
V_{A_STR}	Vstr	Vstr	Vnom
V_{B_STR}	GND	Vstr	Vnom
$CTRL_{STR}$	Vstr_n	GND	Vnom
WL	GND	GND	VDDH

Note: (1) Vstr ≧ VDD, and Vstr_n ≤ − 0.5V.
(2) Vnom = VDD (3) VDDH = 1.2×VDD

diffusion, poly and contact layers intact, and only modify the metal layers to build the ESRO structure (Fig. 5). As shown in Fig. 4(b), two parallel ESROs share the internal connection nodes, and the activation of individual ESRO is decided by the enabling of WL0 or WL1. We then construct an ESRO with one hundred stages of blanked-cells and active-cells (and an Enabling NAND gate) as shown in Fig. 6. The input of the first stage is CN0 node, and the ring is folded every 25-stage. The switch of ring oscillator is placed at the peripheral area

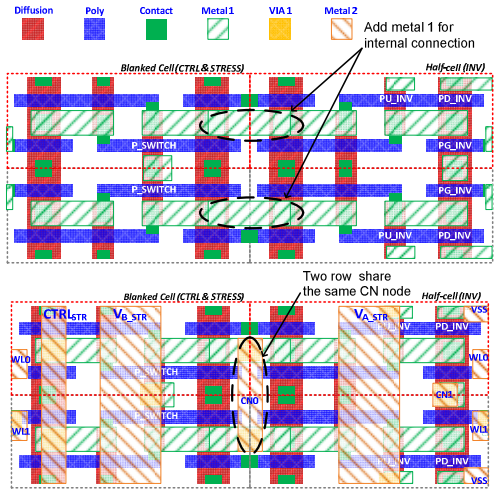

Fig. 5. Modification of 6T cell layout to form ESRO unit-stage.

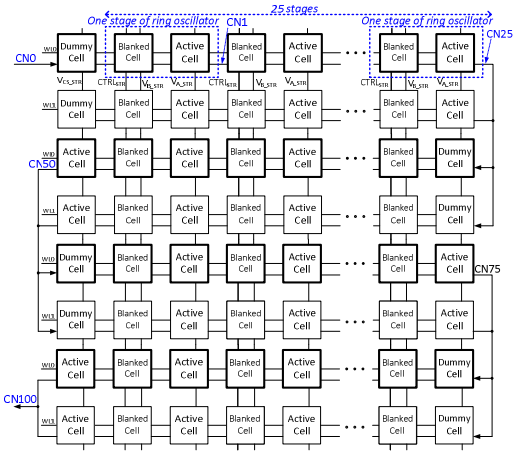

Fig. 6. 100-stage ESRO chain composed of modified SRAM cells.

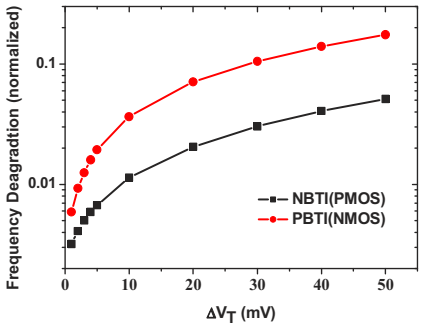

Fig. 7. Simulated frequency degradation vs. threshold voltage drift.

near the ring oscillator array. The dummy cells (CNn (n=0, 25, 50, 75)) used in 100-stage ring array are for passing signals and to preserve the SRAM cell array layout characteristics in each stage of ESRO. The delay time of entire ESRO is 34.5ns. Fig. 7 shows the simulated results of frequency degradation versus threshold voltage drift using modified cell device models. Based on 55nm 1P9M 1.0V SiO_2/poly-gate standard performance CMOS process, the oscillation frequency of ESRO is 14.5 MHz and the area of the two parallel 100 stages ESROs is 546.7 μm^2 (66.67μm*8.2μm), including the dummy

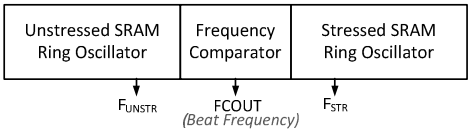

Fig. 8. One set of testing circuits

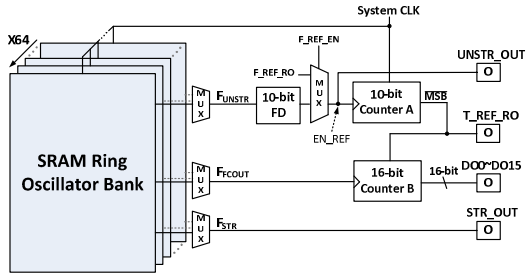

Fig. 9. The counter-based digital read-out measurement scheme.

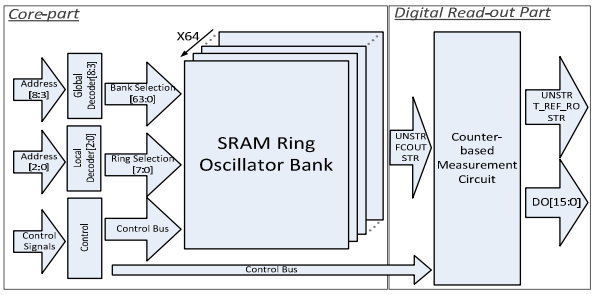

Fig. 10. Block diagram of the whole system.

cells for preserving the layout characteristics of SRAM cell array.

C. *Counter-Based Measurement Circuit*

Since the threshold voltage of MOSFET is an analog signal, it is difficult to extract large amount of data for SRAMs in SOCs. Hence, in this work, we use a full digital scheme to convert the threshold voltage drift to frequency difference to facilitate data extraction, processing, and statistical analysis. A basic set of measurement unit (Fig. 8) consists of two ring oscillators and a frequency comparator [10]. The output of the comparator, F_{FCOUT}, is the "Beat Frequency" (frequency difference between the stressed ring oscillator and the unstressed ring oscillator). The final stage of ESROs, the 101-stage enabling NAND gate, is placed in the frequency comparator block. A counter-based digital read-out scheme is used to convert the beat frequency to digital output. The detailed structure is shown in Fig. 9. With this scheme, we can extract the beat frequency quickly with high resolution.

As shown in Fig. 9, for NBTI in PMOS, the beat frequency F_{FCOUT} ranges roughly from 50 KHz to 760 KHz. Due to wide frequency range of F_{FCOUT}, the counter B (16-bit) should have the ability to cover the lowest and the highest frequency of F_{FCOUT} so that it won't overflow in the counting period, which is decide by counter A (10-bit). The extracted digital data can be easily converted back to threshold voltage drift with a conversion table for statistical analysis.

One SRAM Ring Oscillator bank includes 8 sets of measurement unit. The core part of the measurement circuit (Fig. 9) comprises of 64 SRAM Ring Oscillator banks and some peripheral circuits, such as decoder, global MUX, and buffer. The system block diagram is shown in Fig. 10. The

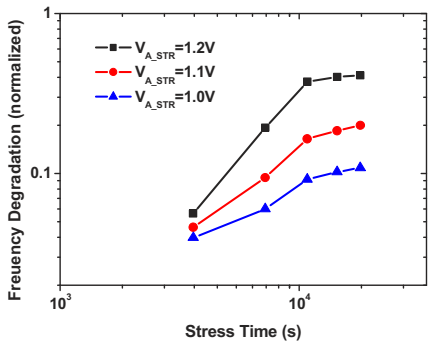

Fig. 11. Measured ESRO frequency degradation versus stress time for different NBTI stress voltage.

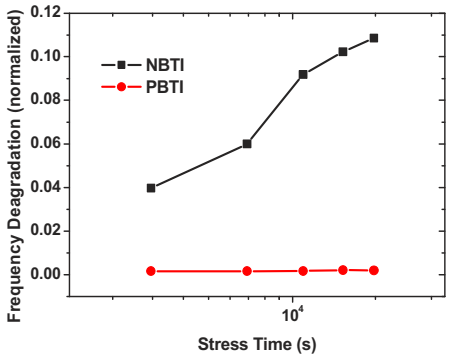

Fig. 12 Measured ESRO frequency degradation under NBTI-only and PBTI-only stress in SiO_2/poly-gate technology.

inputs are 9-bit address and control signals like clock signal (CLK), and enable signal (EN) for ring oscillator. The lowest three bits of address, address [2:0] are for selecting one of the 8-set ESROs and beat frequency circuit in one bank. The [8:3] bits of address are used to select one of the 64 banks. The oscillating signals of F_{STR}, F_{UNSTR} and F_{FCOUT} are transmitted to the digital read-out circuit. STR and UNSTR are also transmitted to the chip output for observation. The area of the overall system, excluding the digital read-out circuit is 1650 um × 1050um. The area of the digital read-out circuit is 903 um^2, representing an area overhead of 0.52%

III. MEASUREMENT RESULTS

A test-chip is implemented in a 55nm SiO_2/poly-gate standard performance bulk CMOS technology. The real-time frequency degradation of stressed ESRO can be observed by recording the counter output or directly observing the STR_OUT in Fig. 9. The external reference signal, F_REF_RO makes the digital read-out circuit more adaptive to wide range of beat frequency.

Fig. 11 shows the measured ESRO frequency degradation versus stress time for NBTI stress voltage of 1.2V, 1.1V and 1.0V. As expected, higher stress voltage, V_{A_STR}, results in larger frequency degradation. We find that the frequency degradation starts to saturate after 10^4 seconds stress time. Based on the frequency degradation vs. threshold voltage drift characteristics in Fig. 7, the threshold voltage drift of pull-up PMOS is more than 50mV after 10^4 seconds of 1.0V stress. Fig. 12 compares the measured results of NBTI stress and PBTI stress. Since SiO_2/poly-gate technology is employed, the ESRO frequency is degraded after NBTI-only stress, while there is negligible change in ESRO frequency after PBTI-only stress. Fig. 13 shows the die photo and layout view for this test chip.

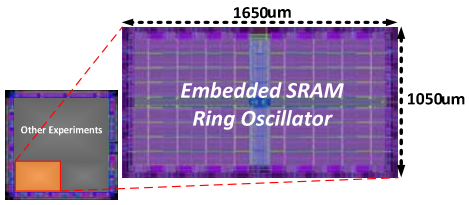

Fig. 13. Die photo (left) and layout view (right) of the test chip.

IV. CONCLUSION

In this work, we present an Embedded SRAM Ring Oscillator (ESRO) structure for measuring the degradation of 6T SRAM cell transistors induced by NBTI/PBTI. The ESRO preserves the original layout characteristics of 6T SRAM cell array with stress capability. We also describe the digital read-out scheme, and the measured BTI frequency degradation in 55nm standard performance CMOS technology.

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