High Efficiency Power Management System for Solar Energy Harvesting Applications

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***Abstract*— A high efficiency power management system for solar energy harvesting applications is proposed. The power management system receives power from photovoltaic (PV) cell and generate different voltage levels which are suitable for SoC integrated regulator applications (such as 1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5.6V for I/O components). The power management system also contains a rechargeable battery which is charged by multi-phase maximum power tracking (MPT) circuitry with the PV cell module. In daytime, the battery is charged by PV cell. In the night, the battery will supply energy to the power management system. With the MPT circuitry, the power of PV cell can be regulated in the maximum power region. The power efficiency of the MPT circuitry is average about 80%~73%. All results are simulated in UMC 90nm CMOS technology model.**

I. INTRODUCTION

In the recent years, the market of portable devices such as notebook, cell phone, PDA and smart phone is grow up rapidly and more new portable products will be developed in the near future. In the developing of portable devices, more and more functions are integrated into a product. At the same time, people concern that whether the product can use for a long time without charging the battery in charge socket.

Previously, an ultra-low voltage power management for energy harvesting applications was developed and worked with a FIR filter [1]. With low output voltage of solar cell, a micro-power management system was proposed [2]. The micro-power management system decide the working frequency of charge pump by the room lighting environment and output the maximum power to load circuitry. An energy harvesting application with micro battery was also implemented [3]. This power management circuit accepts energy from RFID power and thermo generator power and outputs the power to micro battery as energy storage. A battery management system for solar energy applications was developed [4]. The battery management system is used to increase the service life time of the battery.

In this work, we develop a high efficiency power management system that is powered by solar energy and outputs different voltage levels for computation circuitry, memory circuitry, and I/O components, as shown in Fig. 1. The circuit of this system is designed for low power SoC applications. We also propose a multi-phase maximum power tracking circuitry with the PV cell module for regulating the PV cell module in the maximum power region. A switched capacitor (SC) DC-DC converter and a voltage regulator are utilized to supply different voltage levels for dynamic voltage scaling applications. High voltage charge pump and negative voltage charge pump also supply high voltage and negative voltage for overall SoC applications. The detail circuitry is described in Section II. Section III shows the simulation results and Section IV concludes this paper.

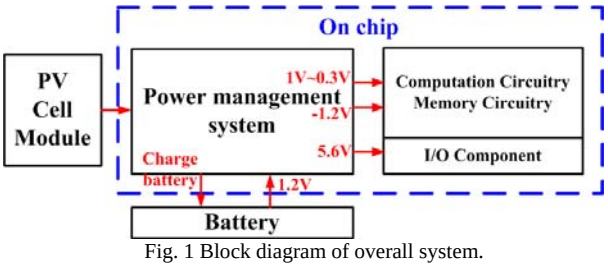


Fig. 1 Block diagram of overall system.

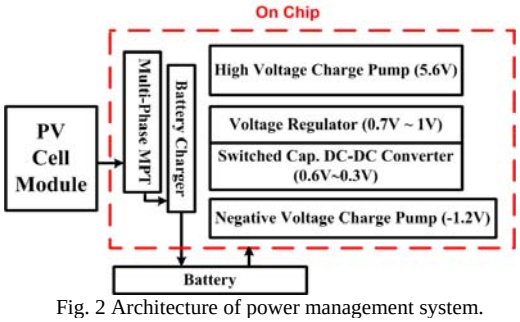


Fig. 2 Architecture of power management system.

II. POWER MANAGEMENT SYSTEM

The proposed power management system is shown in Fig. 2. The power management system contains a PV cell module, a multi-phase maximum power tracking circuitry, a voltage regulator, a SC DC-DC converter, a high voltage charge pump, a battery charger and a negative voltage charge pump.

The maximum power tracking circuitry regulates the PV cell I-V characteristic in the maximum power region instead of arbitrary output voltage. The voltage charger will charge the battery form energy buffer of MPT circuitry. The voltage regulator outputs voltage form 1V~0.7V and the SC DC-DC converter outputs voltage from 0.6V~0.3V which are able to provide the SoC system dynamic voltage. And the high voltage charge pump generates 5.6V for I/O components by utilizing new connection scheme to replace the off-chip capacitors by NMOS capacitors.The PV cell and battery are also implemented in circuit model and simulated with power management system.

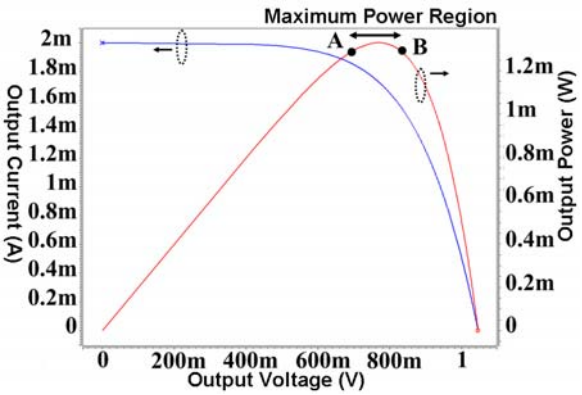


Fig. 3 Power-V and I-V curve of PV cell.

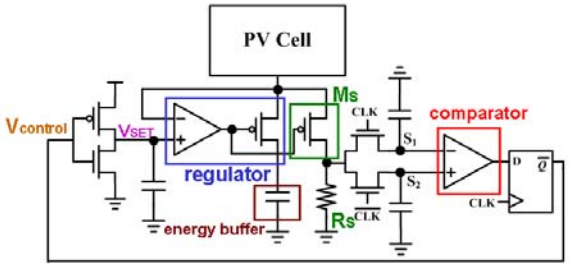


Fig. 4 Schematic of maximum power tracking circuitry.

A. *Tracking progress and maximum power tracking circuitry*

The I-V curve and Power-V curve of PV cell is shown in Fig. 3. The left y-axis is PV cell output current. The right y-axis is PV cell output power. The output voltage of PV cell is between 1V and 0V. The maximum output power of PV cell is 1.32 mW.

The schematic of maximum power tracking circuitry is shown in Fig. 4. As shown in Fig. 3, the MPT circuitry controls V_{SET} and regulates PV cell output current. The corresponding PV cell output voltage is therefore controlled not to exceed point B. So the output power of PV cell will remain in the maximum power region.

The PV cell output current is sensed by M_S and converts current value to voltage value by R_S. And clock controlled switches sample voltage values to store at S_1 and S_2. When PV cell output voltage passes point A shown in Fig. 3, the comparator will detect that S_2 is smaller then S_1 which is over the comparator threshold, and send control signal to reduce V_{SET} for avoiding PV cell output voltage across point B. When the comparator detects that S_2 is larger then S_1, V_{SET} will be increased again and maintain PV cell in maximum power region.

For PV cell module application as shown in Fig.5, the multi-phase MPT circuitry will use multi-phase clocking to average total power of each PV cell. So the PV cell module will supply nearly constant average power. The battery charger will charge the battery by pumping the energy from energy buffer. And the simulation result is shown in Fig. 12 and Fig. 13.

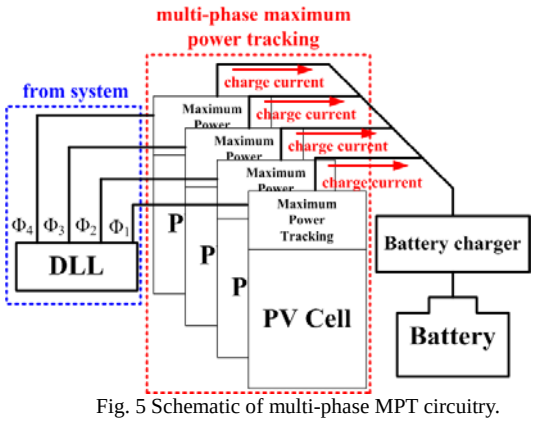


Fig. 5 Schematic of multi-phase MPT circuitry.

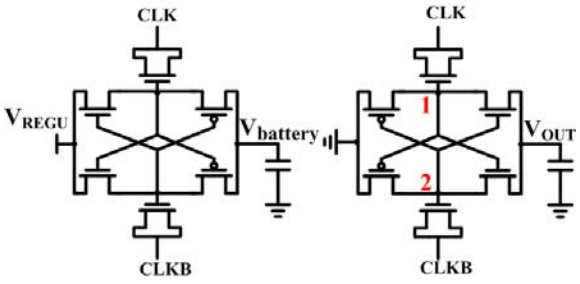


Fig. 6 (a) battery charger. (b) negative voltage generator.

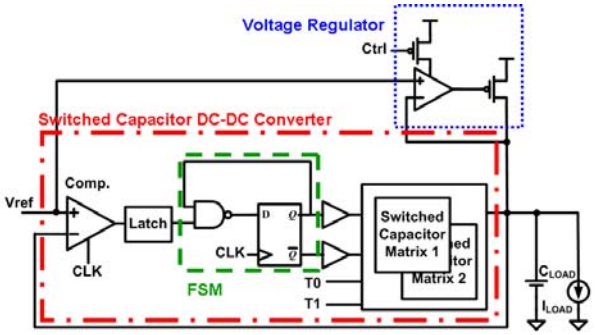


Fig. 7 The voltage regulator and SC DC-DC converter.

B. *Battery Charger and Negative Voltage Generator*

The circuit of battery charger and negative voltage generator is shown in Fig. 6. The battery charger is a voltage doubler. It accepts the supply voltage from MPT circuitry energy buffer and charge the battery. The negative voltage generator accepts ground as input voltage. When CLK is high, the voltage of node 2 is 0V and the voltage of node 1 will be "0". When CLK is low, the voltage of node 1 will be -1.2V and voltage of node 2 will be discharged to 0V. Then, the output voltage will be -1.2V. When CLK is high, the voltage of node 2 will be -1.2V and node 1 is 0V. Thus, the V_{OUT} node will be -1.2V.

C. *Voltage Regulator & Switched Capacitor DC-DC Converter*

The schematic of voltage generator and SC DC-DC converter is shown in Fig. 7. V_{ref} is given by system DAC. When supplying high power operation, voltage regulator will

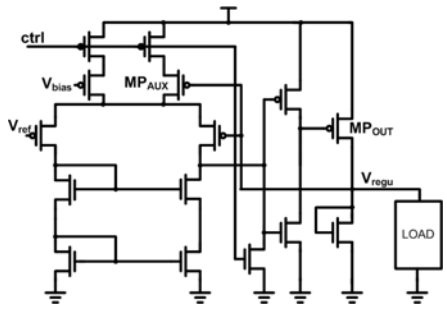
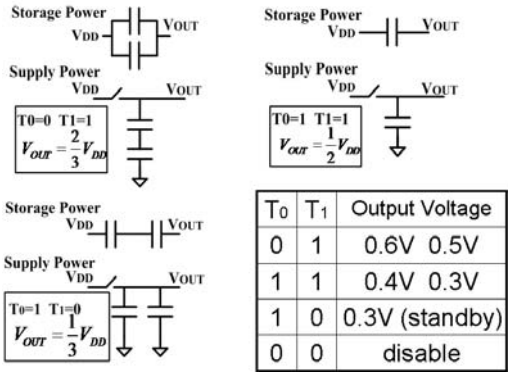


Fig. 8 Circuit of voltage regulator.



T_0	T_1	Output Voltage
0	1	0.6V 0.5V
1	1	0.4V 0.3V
1	0	0.3V (standby)
0	0	disable

Fig. 9 The topology of SC DC-DC converter.

supply 1V~0.7V. The voltage regulator is composed of a differential amplifier, an inverter as a buffer and a power PMOS. The schematics of voltage regulator are shown in Fig. 8. When ctrl is low the voltage regulator is turned on, and ctrl is high the voltage regulator is turn off. As voltage of V_{REGU} node dropping down, the MP_{AUX} will supply more current to differential amplifier. Thus, the MP_{OUT} will turn on rapidly and supply more current to V_{REGU} node. When there is no load current, the MP_{AUX} PMOS will slightly turn on and decrease the consumption power of differential amplifier.

When supplying low power operation, SC DC-DC converter will supply 0.6V~0.3V. The SC DC-DC converter is shown in Fig. 7. T_1 and T_0 are the control signal of switched capacitor topology selection as shown in Fig. 9. When T_1 T_0 =10, the topology output voltage is 2/3 V_{DD} (V_{DD}=1.2V) and supplies 0.5V and 0.6V output voltage. When T_1 T_0 =11, the topology output voltage is 1/2 V_{DD} and supplies 0.4V and 0.3V output voltage. When T_1 T_0 =01, the topology output voltage is 1/3 V_{DD} and supplies 0.3V output voltage for system standby and data retention. When T_1 T_0 =00, the SC DC-DC converter is disabled.

The SC DC-DC converter has two switched capacitor (SC) matrixes. When switched capacitor matrix 1 (SC1) is supplying power to output loading, the switched capacitor matrix 2 (SC2) is storing power from power source. When SC2 is supplying power to output loading, SC1 is storing power from power source. The FSM controls the two SC matrixes, and state diagram of FSM is shown in Fig. 10. When the output voltage is smaller then V_{ref}, the comparator will output high (C=1). If output is high continually, the two SC matrixes will provide energy alternatively. When the output voltage is higher then V_{ref}, the comparator will output low (C=0) and return to S0 state.

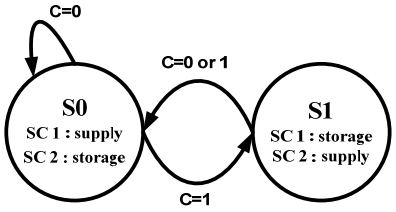


Fig. 10 The stage diagram of finite state machine (FSM).

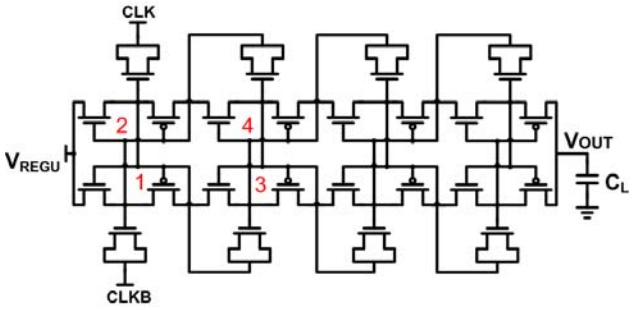


Fig. 11 High voltage charge pump.

D. High voltage Charge Pump

The architecture is based on [5] and replaces the off-chip capacitors by NMOS capacitors. The schematic of high voltage charge pump is shown in Fig. 11.

In this work, the clock generator is supplied by battery voltage source. The initial state is that node 1 = 0V and node 2 = 0V. When CLK is high, the node 1 is 1.2V and node 2 is "1.2V-V_{Tn}". When CLKB is high, the node 2 is "2.4V- V_{Tn}" and the node 1 is 1.2V. As the node CLK is charge to high again, the node 1 is 2.4V. In first stage, the node 1 and node 2 will vibrate between 1.2V and 2.4V. The NMOS capacitors of second stage are connected to node 1 and node 2. Thus the node 3 and node 4 will vibrate between 2.4V and 3.6V. The node VOUT will be 5.6V.

III. SIMULATION RESULTS

To verify the power management system, the design is implemented in UMC 90nm CMOS technology model. The PV cell and battery are also implemented in circuit model and simulated with power management system.

A. Maximum Power Tracking

The first simulation is to verify the function of MPT circuitry. In this simulation the supply current of PV cell provide output current from 2mA to 0mA. The MPT of single PV cell is demonstrated in Fig. 12. As shown in Fig. 12, the PV cell outputs maximum current in the beginning, V_{set} and V_{gate} are increased to decrease the output current for searching the maximum power region of PV cell. When the output current of PV cell is decreased, the output voltage of PV cell increases as shown in Fig. 3. The output current of PV cell is dynamic controlled to maintain PV cell in maximum power region (1.32mW ~ 1.25mW).

Fig. 13 shows the multi-phase MPT with PV cell module. There are four MPT circuitries which are controlled by four different clock phases. The multi-phase control scheme can

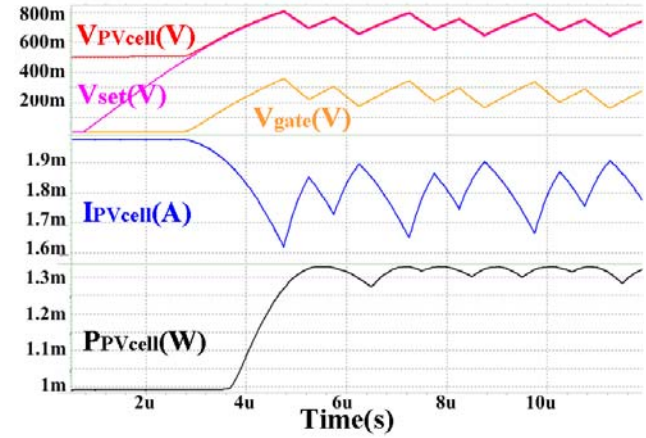


Fig. 12 Single PV cell maximum power tracking transient response.

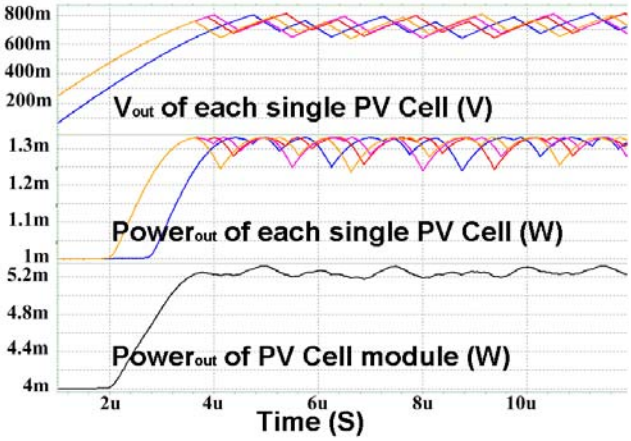


Fig. 13 Multi-phase maximum power tracking for PV cell module.

average the output power ripple. The average output power of PV cell module for each single PV cell is near the maximum power value.

B. Voltage Generation

The voltage generation of voltage regulator, SC DC-DC converter, negative voltage generator and high voltage charge pump are shown in Fig. 14. The voltage regulator and SC DC-DC converter are able to provide voltage form 1V~0.3V. When Ctrl is low, the voltage regulator supplies 1V~0.7V. When Ctrl is high, the SC DC-DC converter supplies 0.6V~0.3V. The negative voltage generator can generate -1.2V and the high voltage charge pump can supply 5.6V. The specifications of power management system is summarized in TABLE I. The system can receive energy from PV cell and generate different voltage for low power SoC applications, and the power efficiency of MPT is about 73%~80%.

IV. CONCLUSIONS

A high efficiency power management system is proposed in this work. The power management system works with PV cell and rechargeable battery. The power management system receives power form PV cell and generates different voltage levels which are suitable for SoC integrated regulator applications. The power management system outputs

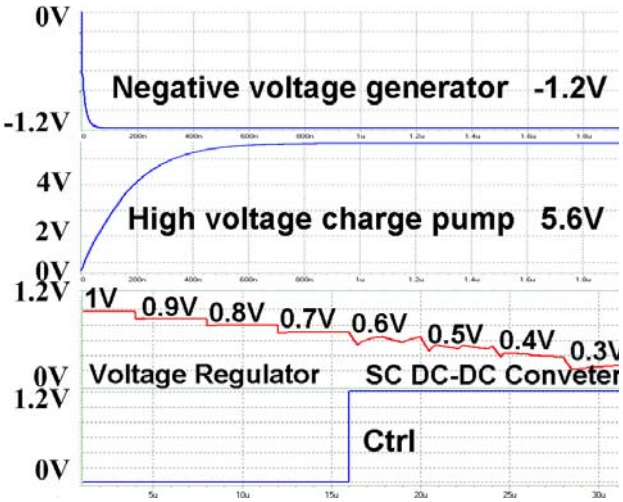


Fig. 14 Voltage generation of overall system

TABLE I
POWER MANAGEMENT SYSTEM FOR SOLAR ENERGY HARVESTING

Technology	UMC 90nm CMOS
Output current of PV cell	2mA~0mA
Output voltage of PV cell	1V~0V
Output power of PV cell	1.32mW~0mW
SC DC-DC converter	0.3V~0.6V
Voltage regulator	1V~0.7V
Negative voltage generator	-1.2V
High voltage charge pump	5.6V
MPT power efficiency	80%~73%

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1V~0.3V for analog circuitry and low power digital circuitry, -1.2V for memory circuitry, and 5.6V for I/O components. The overall system provides a charge method from PV cell and extends the life time of the low power SoC system.

REFERENCES

[1] C. Y. Tsui, H. Shao, W. H. Ki and F. Su, "Ultra-Low Voltage Power Management and Computation Methodology for Energy Harvesting Applications," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 316-319, 2005.

[2] H. Shao, C. Y. Tsui and W. H. Ki,"A Micro Power Management System and Maximum Output Power Control for Solar Energy Harvesting Applications," *ISLPED'07*, pp. 298-303, Aug. 2007.

[3] H. Lhermet, C. Condemine, M. Plissonnier, R. Salot, P. Audebert, and M. Rosset, "Efficient Power management Circuit: From Thermal Energy Harvesting to Above-IC Microbattery Energy Storage," *IEEE Journal of Solid-State Circuits*, vol. 43, No. 1, pp. 246-254, Jan. 2008.

[4] M. Glavin, W. G. Hurley, "Battery management system for solar energy applications," *IEEE Universities Power Engineering Conference*, vol. 1, Sept. 2006, pp. 79-83.

[5] M. -D. Ker, S. –L. Chen, and C.-S. Tsai," Design of Charge Pump Circuit With Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1100-1107, May 2006.