Impact of Gate-Oxide Breakdown on Power-Gated SRAM

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ABSTRACT

This paper presents a detailed analysis on the impacts of various gate-oxide breakdown (BD) paths in column-based header- and footer-gated SRAMs. It is shown that with gate-oxide BD, the RSNM (Read Static Noise Margin) degrades, while the WM (Write Margin) improves in general. The effects of gate-to-source BD of cell transistors are shown to confine to the individual cell, while multiple cells suffering cell transistor drain-to-drain BD in a column could cumulatively affect VVDD (header structure) or VVSS (footer structure), thus influencing other cells in the same column. In particular, we show that the gate-oxide BD of the power-switches have server and even detrimental effects on the margin, stability, and performance of the SRAM array

Index terms: gate-oxide breakdown, power gating technology, SRAM.

I. INTRODUCTION

With technology scaling, the gate-oxide breakdown (BD) has become a major concern in CMOS circuit designs. It is particularly important to understand the impacts of gate-oxide BD on SRAMs as SRAMs occupy most area of a chip and the probability of gate oxide BD is significantly higher than the logic circuits. The leakage from gate-oxide BD exasperates the already poor margin and stability of scaled SRAM cells caused by V_T scatter due to process variation, Random Dopant Fluctuation (RDF), and microscopic effects such as Line Edge Roughness (LER). In addition, most state-of-the-art SRAMs are designed with power-gating structures to reduce leakage in Standby or Sleep mode, and the power-switches can suffer gate-oxide BD as well. Previous papers [1, 2] focused only on a single cell in a normal SRAM architecture. In this paper, we present a detailed analysis on the impacts of gate-oxide BD on power-gated SRAMs. We show that the gate-oxide breakdown of the power-switches have server and even detrimental effects on the margin, stability, and performance of the SRAM array. In the following sections, we first describe the details of our simulation model in PTM CMOS 32nm technology. The Read Static Noise Margin (RSNM) and Write Margin (WM) of cells in a power-gated SRAM under various gate-oxide BD paths are then examined. The impacts of gate-oxide BD on virtual supply lines in Standby or Sleep mode, and the virtual supply bounce during wake-up transition are also analyzed.

This research is supported by National Science Council, R.O.C..

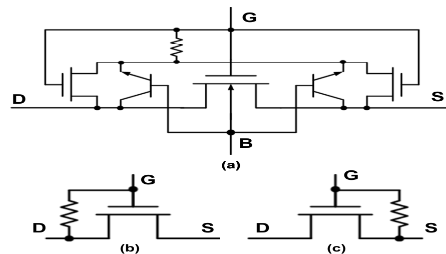

Fig. 1. (a) Equivalent Gate-oxide HBD circuit model. This model can be simplified to (b) when Gate-oxide HBD in drain, (c) when Gate-oxide HBD in source [3].

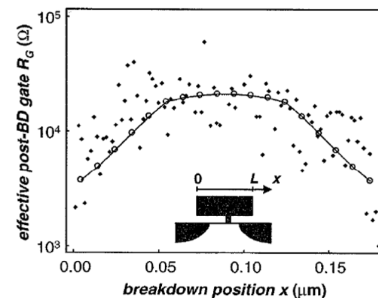

Fig. 2. Effective post-BD resistance vs. BD position [4].

II. POWER-GATED SRAM MODELS

The post-BD characteristics of an NMOS can be explained by the location of a constant-size breakdown path and modeled as a narrow inclusion of highly-doped n-type silicon well with the equivalent circuit shown in Fig. 1 [3]. Under normal operating conditions, the model reduces to simple equivalent resistance paths between the gate and source/drain. The gate leakage current after oxide hard BD can be modeled as I = (1/R)V; where V is the voltage across the gate-oxide, and R is the equivalent post-BD resistance depending on the BD spot area and its position.

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Table I: Possible BD Path Summary

Name	Description	Name	Description
CPS BD	Cell PMOS Gate-to-Source BD	PHS	Header power switch Gate-to-Source BD
CDD BD	Cell Drain-to-Drain BD	PHD	Header power switch Gate-to-Drain BD
CNS BD	Cell NMOS Gate-to-Source BD	PFS	Footer power switch Gate-to-Source BD
CPG BD	Cell pass gate BD	PFD	Footer power switch Gate-to-Drain BD

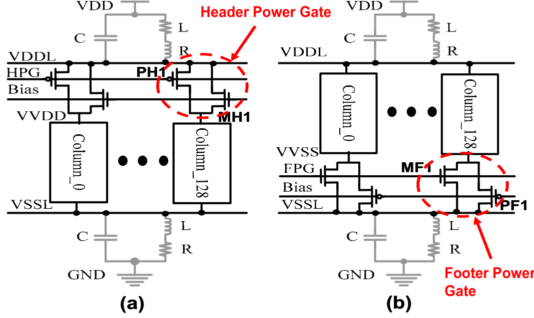

Fig. 3. Power-gated SRAM with (a) header, and (b) footer.

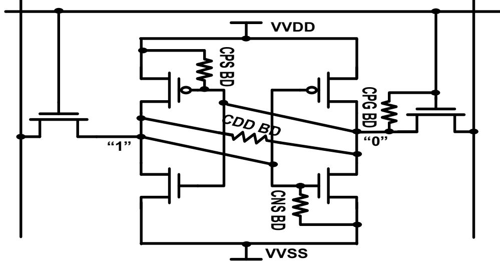

Fig. 4. 6T SRAM with possible BD paths.

The equivalent post-BD resistance becomes smaller when the gate-oxide BD spot position is close to drain or source of a MOSFET (Fig. 2) [4]. Consequently, post-BD gate-to-drain and gate-to-source leakages affect SRAM most significantly. Thus, our analysis focuses on various gate-to-drain and gate-to-source post-BD current paths in the cell and the header/footer power-switches (Table I).

SRAM power-gating structures can be classified into header- and footer-gating structures. Fig. 3(a) shows a column-based header-gated SRAM structure, wherein PH1 is the header power-switch, and MH1 is the clamping device to bias virtual supply (VVDD) for data retention in Standby/Sleep mode. Fig. 3(b) shows a column-based footer-gated SRAM structure. MF1 is the footer power-switch, and PF1 is the clamping device to bias virtual ground (VVSS) for data retention in Standby/Sleep mode. Package model [5] is also included in our analysis, and parasitic capacitance, inductance and resistance of the package are 5.32pF, 8.18nH, and 0.217Ω, respectively. Fig. 4 shows the standard 6T SRAM cells with post-BD leakage paths in our analysis. The SRAM sub-array block size is 128x128 cells.

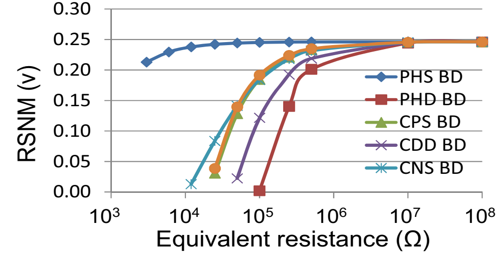

Fig. 5. RSNM vs. post-BD equivalent resistance in a header-gated SRAM.

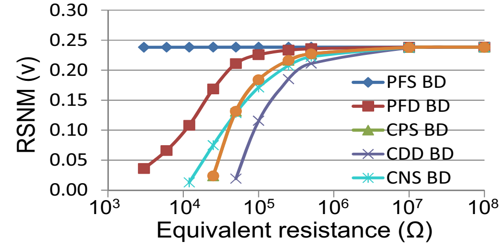

Fig. 6. RSNM vs. post-BD equivalent resistance in a footer-gated SRAM.

The following sections present detailed simulation results based on BSIM Predictive Model PTM 32nm [6]. The SRAM supply voltage is 0.9V. In order to compare impacts of various gate-oxide BD paths, only one gate-oxide BD location/path is considered in each simulation. Table I summarized these gate-oxide BD locations in our analysis. Moreover, the gate-oxide BD is assumed to happen only in one SRAM cell per column in each simulation.

III. READ/WRITE OPERATION

RSNM is defined as the minimum voltage difference between the SRAM inverter trip voltage and the Read disturb voltage induced by voltage divider effect during Read operation. As shown in Fig. 5, RSNM of a header-gated SRAM degrades most when PHD (Header power-switch Gate-to-Drain) BD happens. In contrast, the impact of PHS (Header power-switch Gate-to-Source) BD on RSNM is negligible. The reason is as following: HPG (gate signal of header power-switch) should be "Low" to turn on power-switches to provide sufficient currents for the SRAM array during access cycles. Thus, VVDD decreases seriously when PHD BD happens as it provides a resistive leakage path between the VVDD and the "Low" HPG node, leading to RSNM degradation. On the other hand, when PHS BD happens, its post-BD resistive path shunts the Gate-Source of the power switch, and VVDD is not significantly affected until the post-BD resistance becomes very small. Additionally, RSNM degradation induced by CDD (Cell Drain-to-Drain) BD is worse than that induced by CPS (Cell PMOS Gate-to-Source) BD and CNS (Cell NMOS Gate-to-Source) BD. This is because the SRAM inverter trip voltage decreases and the Read disturb voltage increases at the same time when CDD BD happens. On the other hand, only Read disturb voltage increases when CPS BD happens, while only trip voltage decreases when CNS BD happens. Similar

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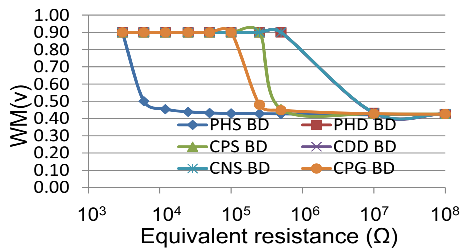

Fig. 7. WM vs. post-BD equivalent resistance in a header-gated SRAM.

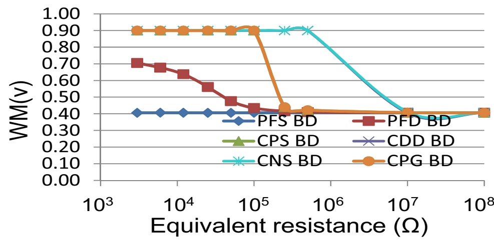

Fig. 8. WM vs. post-BD equivalent resistance in a footer-gated SRAM.

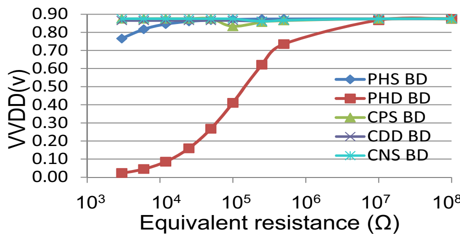

Fig. 9. Active mode VVDD vs. post-BD equivalent resistance in a header-gated SRAM.

RSNM behavior can also be found in a footer-gated SRAM (Fig. 6). The difference is that the post-BD leakage path of a cell plays more important roles than the corresponding cases for header-switches. This is because the NMOS footer-switch is typically stronger than the PMOS header-switch, and the "same" resistive leakage path in NMOS footer would have less effect compared with PMOS header.

WM is defined as the maximum bit-line voltage that can flip the state of a SRAM cell during Write cycles. In the header-gated SRAM, PHD BD, CDD BD, and CNS BD have better WM (Fig. 7). When CDD BD and CNS BD happen, the node storing "High" would be dragged to "Low" easier due to the post-BD leakage path between the node and the node storing "Low" or VVSS. When PHD BD happens, the VVDD is reduced. Thus, WM also improves. On the other hand, in the footer structure, CDD BD and CNS BD have the best WM (Fig .8). This is because the NMOS footer-switch is typically stronger than PMOS header-switch, and the impact of PFD BD in a footer structure is less significant compared with PHD BD in a header structure.

Fig. 9 shows the Active mode VVDD of a header-gated SRAM. The impacts of PHD BD and PHS BD are larger than dd

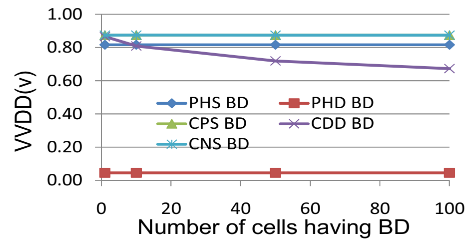

Fig. 10. Active mode VVDD vs. number of cells suff-ering BD with post-BD equivalent resistance of 6KΩ.

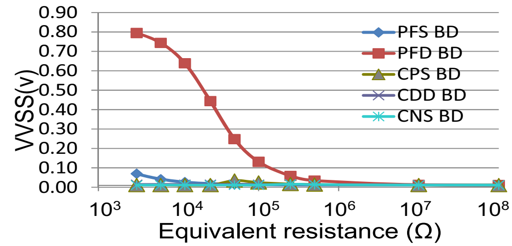

Fig. 11. Active mode VVSS vs. post-BD equivalent resistance in a footer-gated SRAM.

those cases where gate-oxide BD occurs in a cell. The VVDD decrease caused by PHD BD is the most serious because there is a direct post-BD current path between VVDD and the ground ("Low" HPG node). Fig. 10 shows the Active mode VVDD as functions of the number of SRAM cells having gate-oxide BD when the individual BD equivalent resistance is 6KΩ. It shows that with CDD BD, VVDD decreases as more cells suffer gate-oxide BD. On the contrary, for CPS BD and CNS BD, the VVDD is quite independent of the number of cells suffering gate-oxide BD. When CDD BD happens, a current path occurs between two storage nodes of a cell, and the voltage difference between these two storage nodes becomes smaller. The pull-down NMOSs and pull-up PMOSs of the SRAM inverter pairs become weakly turned on, and currents flow through these inverter pairs to Ground. Hence, VVDD decreases with more SRAM cells suffering CDD BD. On the other hand, when CPS BD and CNS BD are serious, data stored in the cell would be flipped (causing error), and there would be no voltage across the gate-oxide leakage path, thus VVDD doesn't decrease. When a cell has one of these two BD locations, it doesn't affect other cells (although its own data may be destroyed). The dependence of Active mode VVSS on gate-oxide BD location in a footer-gated SRAM is shown in Fig. 11. PFD BD causes most increase in VVSS, while the effects of other gate-oxide BD locations are less significant.

IV. Sleep/Standby Mode and Wake-up Transition

When a header-gated SRAM is in Sleep/Standby mode, HPG is "High" to turn off the power-switch and VVDD is biased to proper level by the clamping device for data retention. As shown in Fig. 12, the Sleep/Standby mode VVDD increases significantly with more serious PHD BD, as there is a resistive path between VVDD and HPG (at "High").

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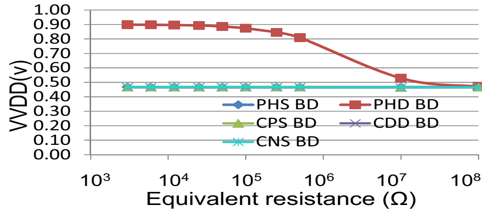

Fig. 12. Sleep mode VVDD vs. post-BD equivalent resistance in a header-gated SRAM.

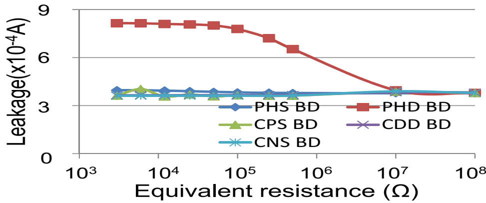

Fig. 13. Sleep mode leakage vs. post-BD equivalent resistance in a header-gated SRAM.

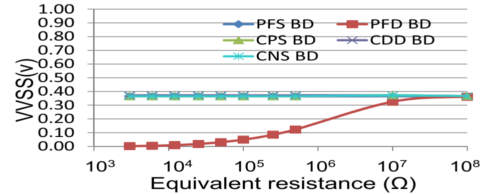

Fig. 14. Sleep mode VVSS vs. post-BD equivalent resistance in a footer-gated SRAM.

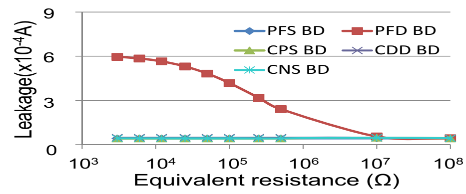

Fig. 15. Sleep mode leakage vs. post-BD equivalent resistance in a footer-gated SRAM.

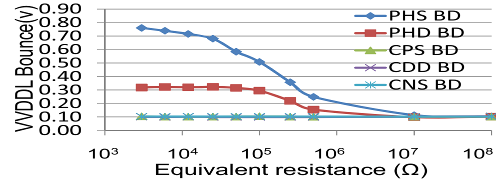

Fig. 16. VVDDL bounce during wake-up vs. post-BD equivalent resistance in a header-gated SRAM.

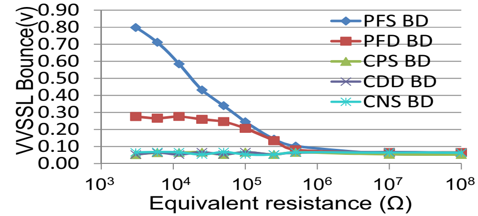

Fig. 17. VVSSL bounce during wake-up vs. post-BD equivalent resistance in a footer-gated SRAM.

Thus, the Sleep/Standby leakage increases significantly (Fig. 13), and the power-gating structure loses its effectiveness. The effects of other gate-oxide BD locations are negligible. Similarly, when a footer-gated SRAM is in Sleep/Standby mode, FPG is "Low" and VVSS is biased by the clamping device to proper level for data retention. PFD BD causes VVSS to decrease significantly (Fig. 14), and footer-gating structure loses its ability to reduce Sleep/Standby leakage with serious PFD BD (Fig. 15).

When the SRAM wakes up from Sleep/Standby mode, the power-switch turns on, and large wake-up current flows through parasitic capacitance, inductance, and resistance of the package, thus inducing supply line (node VDDL or VSSL in Fig. 3) and virtual supply line (VVDD or VVSS) bounce. In the header-gated structure, PHS BD and PHD BD induce significant VDDL bounce (Fig. 16). This is because their post-BD current paths decrease the equivalent resistance of the power-switch. Similar behavior can be observed for VSSL bounce in the footer-gated structure (Fig. 17).

V. Conclusions

We have investigated impacts of various gate-oxide BD paths on column-based header- and footer-gated SRAMs based on BSIM PTM 32 nm node. It was shown that with gate-oxide BD, the RSNM degraded while the WM improved in general. Although stored data could be flipped, CPS BD and CNS BD in individual cell won't affect other cells. In contrast, if there were multiple cells suffering CDD BD in a column, their impacts on VVDD (header structure) or VVSS (footer structure) would be cumulative and would affect other cells in the same column. Most important, we showed that gate-oxide breakdown of the power-switch caused significant degradation of the cell stability and margin, and could lead to the detrimental collapse of the Active mode supply across the array (thus affecting the functionality of the entire array), large increase of Sleep/Standby voltage across the array (thus increasing the leakage and negating the effectiveness of power-gating), and unacceptable virtual supply bounce during wake-up.

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