Logical Effort Models with Voltage and Temperature Extensions in Super-/Near-/Sub-threshold Regions

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***Abstract*—The voltage-/temperature-induced delay estimation error of conventional logical effort is much more severe in near-/sub-threshold region. In this paper, super-/near-/sub-threshold logical effort models are proposed to eliminate delay estimation error caused by voltage and temperature variations. These models establish over the four different nanoscale CMOS generations. They also take environmental parameter variations with wide supply voltage 0.1~1V and full temperature -50~125ºC range into account. The simulation results are using UMC 90-nm, PTM 65-, 45- and 32-nm bulk CMOS technologies, respectively. The average absolute error among the three regions are only 6.01%, 4.12%, 8.01% and 6.55% for UMC 90-nm, PTM 65-, 45- and 32-nm technology, respectively. Proposed models extend the original high performance circuits design in super-threshold region to low power circuit design in near-threshold and sub-threshold regions. They are useful for future green electronics applications.**

I. INTRODUCTION

Power becomes the dominant design constraint in many emergence applications such as mobile consumer electronics or wireless sensor networks. The techniques of ultra-low voltage (ULV) design have been exploded continuously. In addition, the minimum energy point appeared at the voltage where transistors operate in weak-inversion (also called sub-threshold region) [1], [2]. However, sub-threshold circuits are much more sensitive to environmental variations than super-threshold ones. Recently, three-dimensional integrated circuit (3D-IC) technology is developed for overcoming the barriers in large interconnections. The high integration of 3D-IC introduces hot spot problem because of different thermal distribution. The temperature inconsistency brings performance coherence problem in ULV circuits design. Voltage and temperature variations affect timing behavior of logic gates significantly with lower voltage and advanced CMOS technology. They may lead to functional errors in digital circuits. Therefore, novel unified logical effort models for optimizing of combinational logic by considering temperature and voltage variations are proposed.

The logical effort model proposed by Sutherland, Sproull, and Harris in 1999 is a method for estimating circuit path delay [3]. By using logical effort, it is easy to estimate path delay from simple calculation, but it doesn't consider environmental conditions. Many papers have been presented to improve the accuracy of logical effort model in different conditions. The effect of a linear input transition time was introduced [4]. A subthreshold logical effort was presented for optimal subthreshold device sizing [5]. However, the effects of voltage and temperature variations are not considered. I/O coupling capacitance and the input ramp effect on logical effort was considered [6]. The influences of voltage and temperature on logical effort were introduced in UMC 90nm bulk CMOS process [7], which logical gates, however, were operated in strong inversion region.

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In this paper, strong-/moderate-/weak-inversion logical effort models for different CMOS operation regions are proposed. The formulas of logical effort models will be derived in section II. Section III shows the comparisons of logical effort models in super-/near-/sub-threshold regions and simulated delay. Finally, we conclude this work in section IV.

II. STRONG-/MODERATE-/WEAK-INVERSION LOGICAL EFFORT MODELS

The logical effort models in super-/near-/sub-threshold regions are derived by considering current equation of physical alpha-power law [8] and conventional logical effort model simultaneously. In logic gates, the operation region of MOSFET is determined by the value of supply voltage. When the supply voltage is less than threshold voltage ($V_{DD} < V_T$), then the weak-inversion (or sub-threshold) current is derived as

$$I_{DSUB} = (W/L)\mu_0 C_{OX} \frac{\eta}{\beta^2} \exp[(\beta/\eta)(V_{DD} - V_T - \eta/\beta)], \quad (1)$$

where (W/L) is the channel width-to-length ratio, C_{OX} is the gate oxide capacitance per unit area, μ_0 is carrier mobility, and the MOSFET parameters

$$\beta = q/(kT), \quad \eta = 1 + C_{D0}/C_{OX}. \quad (2)$$

When supply voltage is applied near threshold voltage ($V_{DD} \sim V_T$), velocity saturation is negligible ($E_C L >> V_{DD} - V_T$),

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Strong-inversion (Super-threshold):

$$I_D = 2(W/L)C_{OX}\mu_{eff}(E_C L/\eta)^{1/2}(V_{DD}-V_T)^{3/2}$$

Moderate-inversion (Near-threshold):

$$I_D = (W/L)C_{OX}\mu_{eff}(1/\eta)(V_{DD}-V_T)^2$$

Weak-inversion (Sub-threshold):

$$I_D = (W/L)\mu_0 C_{OX}\frac{\eta}{\beta^2}\exp[(\beta/\eta)(V_{DD}-V_T-\eta/\beta)]$$

Figure 1. Simplified physical alpha-power law current equations

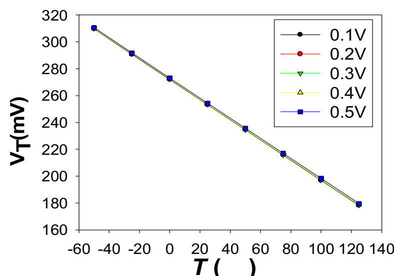

Figure 2. V_T - T plot with gate voltage 0.1~0.5V (UMC 90-nm)

This region is called moderate-inversion (near-threshold) region. Thus, we simplify the saturation voltage and I_{DSAT} from [8] and obtain

$$V_{DSSAT}\,|\,E_C L \gg V_{DD}-V_T \approx (1/\eta)(V_{DD}-V_T)\,, \tag{3}$$

$$I_{DSAT}\,|\,E_C L \gg V_{DD}-V_T = (W/L)C_{OX}\mu_{eff}(1/\eta)(V_{DD}-V_T)^2\,. \tag{4}$$

When supply voltage is applied much larger than threshold voltage ($V_{DD} >> V_T$), strong velocity saturation ($E_C L<<V_{DD} - V_T$) is reached. This is called strong-inversion (super-threshold) region. Again, we simplify the saturation voltage and I_{DSAT} from [8] as

$$V_{DSSAT}\,|\,E_C L \ll V_{DD}-V_T = [(2E_C L/\eta)(V_{DD}-V_T)]^{1/2}\,, \tag{5}$$

$$I_{DSAT}\,|\,E_C L \ll V_{DD}-V_T \approx 2(W/L)C_{OX}\mu_{eff}(E_C L/\eta)^{1/2}(V_{DD}-V_T)^{3/2}\,. \tag{6}$$

All three regions of MOS current are derived in (1), (4) and (6), summarized in Fig. 1. To modify the logical effort model, the logical effort g can be derived with drain current I_D. In the original logical effort model, the delay can be expressed as

$$d_{abs} = \tau(f+p) = \tau(gh+p) \tag{7}$$

d_{abs} is absolute delay; τ is unit delay of an inverter template; f, g, h and p are stage effort, logical effort, fanout and parasitic delay respectively. The definitions of τ, g, h, and p

$$\tau = \kappa R_{inv}C_{inv}\,,\; g = \frac{R_t C_{int}}{R_{inv}C_{inv}}\,,\; h = \frac{C_{out}}{C_{in}}\,,\; p = \frac{R_t C_{pt}}{R_{inv}C_{inv}} \tag{8}$$

where R_{inv} and C_{inv} are output resistance and input capacitance of an inverter template; R_t, C_{int}, C_{pt} are output resistance, input capacitance and output parasitic capacitance of a specific gate.

In (8), logical effort is equal to the ratio of gate RC to inverter RC

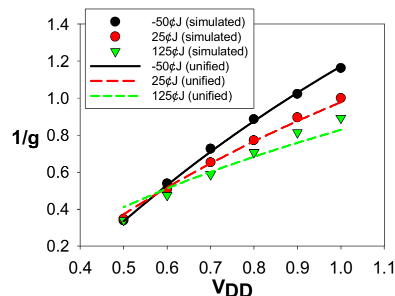

Figure 3. 1/g in process UMC 90-nm (strong-inversion).

TABLE I. FUNCTION *A(T)* FOR STRONG-INVERSION

	A(T)
UMC 90nm	$1.77\times10^{-5}T^2 - 6.75\times10^{-3}T + 1.67$
PTM 65nm	$4.83\times10^{-5}T^2 - 1.63\times10^{-2}T + 2.30$
PTM 45nm	$7.32\times10^{-5}T^2 - 2.25\times10^{-2}T + 2.93$
PTM 32nm	$5.99\times10^{-5}T^2 - 1.81\times10^{-2}T + 2.30$

$$g = \frac{R_t C_{int}}{R_{inv}C_{inv}} = kR_t C_{int} = k\frac{V_{DD}}{I_D}C_{int}\,. \tag{9}$$

The inverter $1/R_{inv}C_{inv}$ is equal to constant k, and R_t is equal to V_{DD}/I_D, where I_D is drain current. The inverse of logical effort

$$1/g = \frac{I_D}{kV_{DD}C_{int}}\,. \tag{10}$$

From (10), inverse of logical effort is proportional to I_D; there are three regions for I_D as well as g: strong-, moderate- and weak-inversions. The driving ability of NMOS and PMOS are not the same in different regions. The inverter sizing ratios Wp/Wn, are set as 2.5, 2.0 and 1.5 in strong-, moderate- and weak-inversion regions to get balanced rise and fall delay. Because of the manuscript length limitation, figures of 1/g will only be shown in UMC 90-nm.

A. Strong-inversion (Super-threshold) Region

In strong-inversion region, MOSFET operates with strong carrier velocity saturation. Substitute I_D (6) into (10)

$$\begin{aligned} 1/g &= \frac{(W/L)C_{OX}\mu_{eff}(2/\eta)^{1/2}(E_C L)^{1/2}(V_{DD}-V_T)^{3/2}}{kV_{DD}C_{in}} \\ &= const1\cdot\mu_{eff}\frac{(V_{DD}-V_T)^{3/2}}{V_{DD}} \end{aligned}\,, \tag{11}$$

where *const1* represents all constant coefficients. From Fig. 2, V_T can be expressed as $V_{T0} - aT$ where V_{T0} stands for threshold voltage at 0 ºC; Unified *1/g* function is curve fitted by

$$1/g_u = A(T)\frac{(V_{DD}-V_{T0}+aT)^{3/2}}{V_{DD}}\,. \tag{12}$$

g_u stands for unified logical effort; *A(T)* is two-degree polynomial of T. By measuring logical effort with various V_{DD} and T, *A(T)* is solved and listed in TABLE I. In this region, we set g equal to 1 at V_{DD} = 1V, T = 25 ºC and the V_{DD} range is from 0.5V to 1.0V. Fig. 3 shows unified and simulated *1/g* value to various V_{DD} and T. The average absolute error are

TABLE II. FUNCTIONS $B(T)$, $C(T)$ AND $D(T)$ FOR MODERATE-INVERSION

	$B(T)$	$C(T)$	$D(T)$
UMC 90nm	$4.76\times10^{-4}T^2 - 9.20\times10^{-2}T + 84.7$	$-3.94\times10^{-4}T^2 + 6.91\times10^{-2}T - 2.35$	$7.39\times10^{-5}T^2 - 1.11\times10^{-2}T + 6.87\times10^{-2}$
PTM 65nm	$5.09\text{x}10^{-4}T^2 - 1.96\text{x}10^{-1}T + 26.0$	$-3.36\text{x}10^{-4}T^2 + 1.29\text{x}10^{-1}T - 15.5$	$5.49\text{x}10^{-5}T^2 - 2.10\text{x}10^{-2}T + 2.39$
PTM 45nm	$1.16\text{x}10^{-3}T^2 - 3.20\text{x}10^{-1}T + 36.0$	$-8.37\times10^{-4}T^2 + 2.27\times10^{-1}T - 23.7$	$1.51\text{x}10^{-4}T^2 - 4.01\text{x}10^{-2}T + 4.00$
PTM 32nm	$1.25\times10^{-3}T^2 - 3.75\times10^{-1}T + 42.8$	$-8.93\times10^{-4}T^2 + 2.70\text{x}10^{-1}T - 29.3$	$1.59\text{x}10^{-4}T^2 - 4.87\text{x}10^{-2}T + 5.11$

TABLE III. FUNCTIONS $E(T)$ AND $F(T)$ FOR WEAK-INVERSION

	$E(T)$	$F(T)$
UMC 90nm	$1.16\times10\text{-}09T^4 - 2.35\times10\text{-}07T^3 + 5.64\times10\text{-}06T^2 + 6.35\times10\text{-}03T + 4.67\times10\text{-}01$	$2.36\times10\text{-}04T^2 - 1.02\times10\text{-}01T + 2.18\times10\text{+}01$
PTM 65nm	$7.51\times10\text{-}10T^4 - 1.46\times10\text{-}07T^3 - 1.06\times10\text{-}06T^2 + 1.20\times10\text{-}03T + 1.02\times10\text{+}00$	$2.11\times10\text{-}04T^2 - 9.13\times10\text{-}02T + 2.22\times10\text{+}01$
PTM 45nm	$6.47\times10\text{-}10T^4 - 1.44\times10\text{-}07T^3 + 3.09\times10\text{-}06T^2 + 1.15\times10\text{-}03T + 9.89\times10\text{-}01$	$2.08\times10\text{-}04T^2 - 9.39\times10\text{-}02T + 2.20\times10\text{+}01$
PTM 32nm	$3.29\times10\text{-}10T^4 - 1.17\times10\text{-}07T^3 + 1.08\times10\text{-}05T^2 + 7.29\times10\text{-}04T + 9.59\times10\text{-}01$	$1.80\times10\text{-}04T^2 - 8.95\times10\text{-}02T + 2.12\times10\text{+}01$

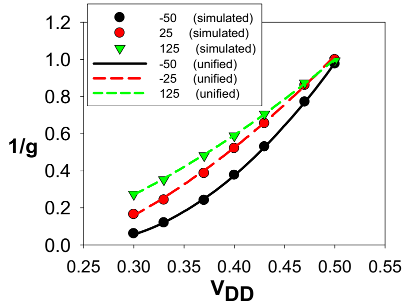

Figure 4. 1/g in process UMC 90-nm (moderate-inversion).

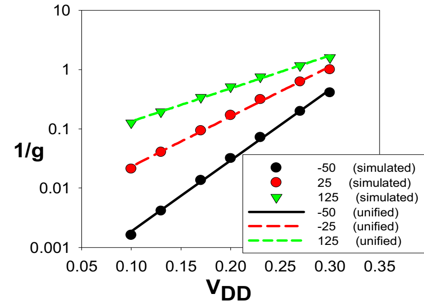

Figure 5. 1/g in process UMC 90-nm (weak-inversion).

3.89%, 4.12%, 8.01%, 6.55% for unified logical effort in UMC 90-nm, PTM 65-, 45- and 32-nm.

B. Moderate-inverasion (Near-threshold) Region

In moderate-inversion region, MOSFET operates with negligible carrier velocity saturation. Substitute I_D (4) into (10)

$$1/g = \frac{(W/L)C_{OX}\mu_{eff}(1/\eta)(V_{DD}-V_T)^2}{kV_{DD}C_{int}} = const2\cdot\frac{\mu_{eff}(V_{DD}-V_{T0}+aT)^2}{V_{DD}} \quad (13)$$

where *const2* represents all const coefficients. V_T is function of *T*. Unified *1/g* is curve fitted by

$$1/g_u = B(T)V_{DD}^2 + C(T)V_{DD} + D(T)\,. \quad (14)$$

g_u stands for unified logical effort; *B(T)*, *C(T)*, and *D(T)* are two-degree polynomial of *T*. By measuring logical effort with various V_{DD} and *T*, *B(T)*, *C(T)*, and *D(T)* are solved, listed in TABLE II. In this region, *g* is set to be 1 at V_{DD} = 0.5V, T = 25 ºC and the V_{DD} range is from about 0.3V to 0.5V. The divide points between moderate- and weak-inversions are 0.3V, 0.33V, 0.34V, 0.35V in UMC 90-nm, PTM 65-, 45- and 32-nm. Fig. 4 is unified and simulated *1/g* value to various V_{DD} and *T*. The average absolute error are 1.52%, 1.20%, 1.44%, 5.04% for unified logical effort in UMC 90-nm, PTM 65-, 45- and 32-nm.

C. Weak-inversion (Sub-threshold) Region

In weak-inversion region, MOSFET operates in sub-threshold mode. Substitute I_D (1) into (10)

Strong-inversion (Super-threshold):

$$1/g_u = A(T)\frac{(V_{DD}-V_{T0}+aT)^{3/2}}{V_{DD}}$$

Moderate-inversion (Near-threshold):

$$1/g_u = B(T)V_{DD}^2 + C(T)V_{DD} + D(T)$$

Weak-inversion (Sub-threshold):

$$1/g_u = E(T)\exp\{F(T)[V_{DD}-V_{T0}]\}$$

Figure 6. Unified logical effort models

$$1/g = \frac{(W/L)\mu_0 C_{OX}\dfrac{\eta}{\beta^2}\exp[(\beta/\eta)(V_{GS}-V_T-\eta/\beta)]}{kV_{DD}C_{in}} = const3\cdot\mu_0\frac{\exp[(\beta/\eta)(V_{GS}-V_{T0}+aT-\eta/\beta)]}{V_{DD}}, \quad (15)$$

where *const3* represents constant coefficients, β and V_T are functions of *T*. Unified *1/g* is curve fitted by

$$1/g_u = E(T)\exp\{F(T)[V_{DD}-V_{T0}]\}. \quad (16)$$

g_u stands for unified logical effort; *E(T)* is a four-degree polynomial of *T*, and *F(T)* is a two-degree polynomial of *T*. By measuring 1/g with various *T* and V_{DD}, *E(T)* and *F(T)* can be calculated, listed in TABLE III. In this region, *g* is set to be 1 at T = 25 ºC, and V_{DD} = 0.3, 0.33, 0.34, 0.35V for UMC 90-nm, PTM 65-, 45- and 32-nm. Fig. 5 is unified and simulated *1/g* value with various V_{DD} and *T*. The average absolute error are 6.01%, 3.03%, 2.97%, 5.14% for unified logical effort in UMC 90-nm, PTM 65-, 45- and 32-nm. The average absolute error of unified logical effort is listed in TABLE IV. The unified logical effort models are summarized in Fig. 6.

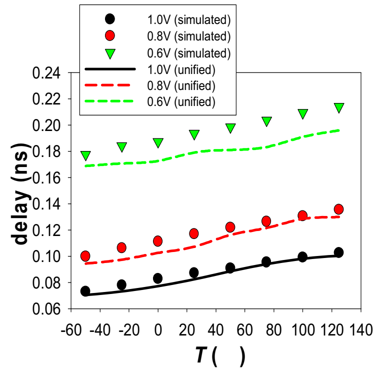

Figure 8. d_{gates} in UMC 90(strong-inversion)

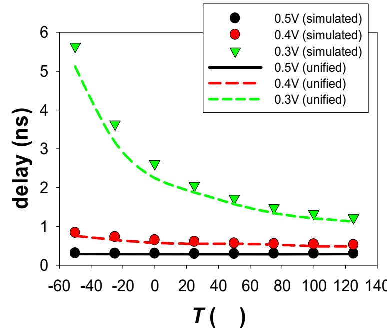

Figure 9. d_{gates} in UMC 90(moderate-inversion)

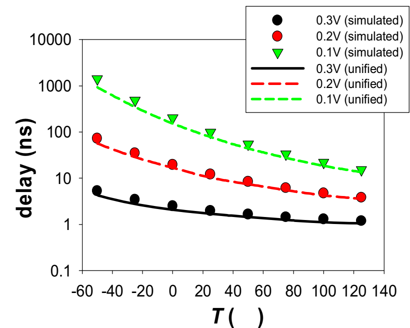

Figure 10. d_{gates} in UMC 90(weak-inversion)

TABLE IV. LOGIC EFFORT MODELING ERROR

Average Absolute Error	Strong-inversion	Moderate-inversion	Weak-inversion
UMC 90nm	3.89%	1.52%	6.01%
PTM 65nm	4.12%	1.20%	3.03%
PTM 45nm	8.01%	1.44%	2.97%
PTM 32nm	6.55%	5.04%	5.14%

TABLE V. RATIO OF LOGICAL EFFORT FOR LOGIC GATES

	Strong-inversion	Moderate-inversion	Weak-inversion
Wp/Wn	2.5	2.0	1.5
g (INV)	g_u	g_u	g_u
g (2-NAND)	g_u×9/7	g_u×4/3	g_u×7/5
g (2-NOR)	g_u×12/7	g_u×5/3	g_u×8/5

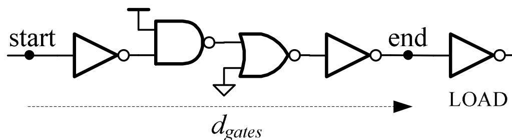

Figure 7. A test vehicle for proposed logical effort models

III. SIMULATION RESULTS

In this section, the test vehicle shown in Fig. 7 composes of inverters, 2-input NAND and NOR gates. It is used to evaluate proposed universal logical effort models. The delay of logic gates are affected by environmental condition. The proposed logical effort models in (12), (14) and (16) can rapidly predict the delay with voltage and temperature variations. The logical effort of 2-input NAND and NOR are extended following classic logic effort rule. Their logic effort, listed in TABLE V, can be derived from different Wp/Wn ratio in three distinct regions. We estimate test vehicle delay d_{est} by classic delay equation:

$$d_{est} = \tau \times \sum (f + p) = \tau \times \sum (g \times h + p). \quad (17)$$

The comparisons of delay between estimation by (17) and simulation are shown in Fig. 8, 9 and 10. τ is absolute delay of a unit size inverter at the specific T and V_{DD}. The average absolute delay estimation error in the test vehicle are 12.6%, 7.96% and 16.8% in strong-, moderate- and weak-inversions. With the established logical effort models, the delay of one circuit path can easily and accurately be predicted, and the effects of voltage and temperature variations are also included.

IV. CONSLUSION

In ULV design, temperature and voltage variations severely affect timing behavior of logic gates. Compared with conventional logical effort model, proposed strong-/moderate-/weak-inversion logical effort models consider wide voltage and temperature variations; by establishing proposed logical effort models beforehand, the delay of one circuit path can be estimated quickly. There are three regions in the proposed models for different MOSFET operation states: super-, near- and sub-threshold regions. Also, they have been established in processes UMC 90-nm, PTM 65-, 45- and 32-nm. The maximum average absolute error is 8.01% for logical effort, and 16.8% for the delay estimation in the test vehicle.

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