Low Quiescent Current Variable Output Digital Controlled Voltage Regulator

Wei-Chih Hsieh and Wei Hwang
Department of Electronics Engineering & Institute of Electronics, and
Microelectronics and Information Systems Research Center,
National Chiao Tung University, Hsin-Chu 300, Taiwan
wesleyhs.ee93g@nctu.edu.tw

***Abstract*—In this paper, a digital controlled push-pull linear voltage regulator is proposed. The designed regulator can provide a variable output voltage ranging from 0.5V to 1V in steps of 0.1V. It can supply a maximum of 100mA for each output level. A time interleaving control technique is also presented to enhance the output performance. By using UMC 65nm standard CMOS technology, the ripple of the output voltage when the load or output level changes is smaller than 10% of each specific output level. The current efficiency is 99.9% with only 126μA quiescent current.**

I. Introduction

The capability of providing multiple supply voltages is the key for dynamic voltage frequency scaling (DVFS) [1] to success. Typically, a switching dc-dc converter [2] is used to serve the objective. The power efficiency of the switching dc-dc converters can be as high as 95%. However, the required large inductors and capacitors which occupy huge chip area are unattractive for system integration.

Linear regulators [3]–[7] are the other category of voltage converters. The theoretical maximum power efficiency of a linear regulator is inherently limited by its input-output voltage property. Compared to switching converters, linear regulators are much easier to be integrated on-chip without area consuming inductors. The standby power, i.e., the quiescent current, is also lower. Conventionally linear regulators use analog building blocks [3]–[6]. As shown in Fig. 1, an analog error amplifier compares the regulated output with the reference voltage. An analog buffer drives the output device which have a large gate capacitance. The quiescent current of a linear regulator is desired to be as small as possible to keep an acceptable power efficiency. However, the demand of small quiescent current slows down the transient response of analog circuit. The analog circuit building blocks also suffer from voltage scaling and technology advancing. The voltage scaling results in decreasing voltage drop across each stacked transistor in the analog circuit that causes slower response. The increasing variations because of technology advancing make devices matching that is important for analog circuit more difficult. Moreover, the well-known drawback of the analog circuit blocks is the difficulty of technology migration.

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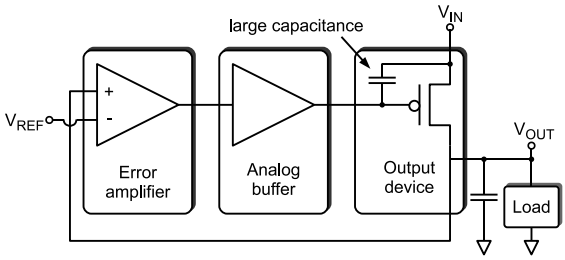


Fig. 1. Conventional analog style linear regulator [7].

On the other hand, digital circuits have some advantages over analog circuits. Digital circuit consumes very little current in steady state and provides large output current when switching. It functions well as the supply voltage decreases. The digital circuit is also easy to migrate from one technology to another. There had been a digital controlled linear regulator [7] in literature. The error amplifier was constructed by inverter based amplifier. The output of the error amplifier was then digitized for digital processing. The technique drew 25.7mA quiescent current that was large.

In this paper, a fully digital controlled linear voltage regulator is proposed to overcome the aforementioned issues of analog circuits. The idea is to replace the analog building blocks in Fig. 1 with their digital counterparts. The quiescent current is low and the output voltage can be altered to meet the requirement of DVFS technique.

The architecture of the proposed digital controlled linear regulator is presented in Section II. The time interleaving control strategy to enhance the transient response of the digital control loop is described in Section III. Section IV makes some more remarks on the proposed digital controlled voltage regulator. And Section V summarizes this paper.

II. Digital Controlled Voltage Regulator

The architecture of the proposed digital controlled linear regulator is presented in Fig. 2. Push-pull topology as in [4] is used to avoid drawing an extra quiescent current in no load condition. Instead of using an error amplifier [7], the regulated and the reference voltages are digitized by two analog-to-digital converters (ADC) and then compared digitally. These

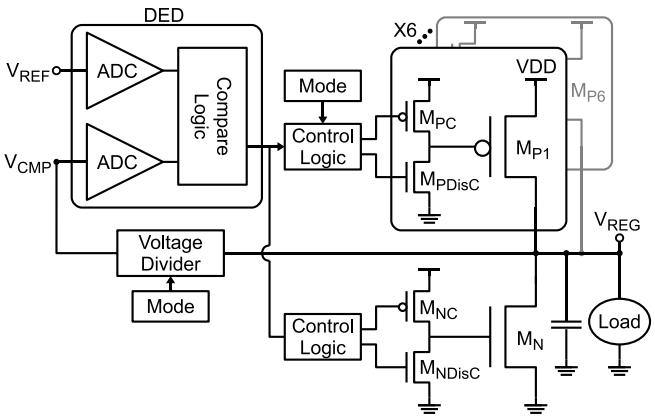


Fig. 2. Block diagram of proposed digital controlled linear regulator.

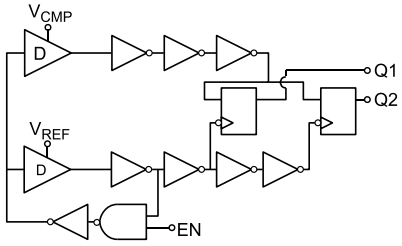


Fig. 3. Block diagram of the digital error detection (DED) block.

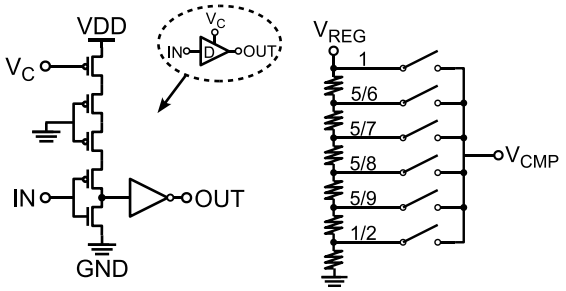
logics are mentioned as a digital error detection (DED) block in the following. The control system independently charges/discharges the gates of push and pull devices based on the result of DED. The proposed regulator provides a variable output voltage ranging from 0.5V to 1V in steps of 0.1V. The reference voltage is assumed to be 0.5V. The voltage divider divides the regulated voltage to around 0.5V when it is higher than that. The divided voltage is therefore able to be compared with the reference voltage.

The driving strength of the push device varies as the regulated voltage changes because of different V_{DS}. In order to reduce the charging/discharging power on the gate of output devices, the output devices are divided into six groups, M_{P1} to M_{P6} as shown in Fig. 2. These groups are accumulated to supply 100mA load current for each output regulated voltage level. The mode control block controls the activation of the charging/discharging circuits of each group according to the output voltage setting.

Delay line based ADC is chosen in this work because of its digital implementation. Typical delay line based ADC uses a long delay line to have a good resolution. For example, an 1ns delay line was reported [8]. In this work, a short delay line including one voltage controlled delay cell and several inverters for waveform shaping is used to have a fast control loop response. The block diagram of DED is shown in Fig. 3 whereas the schematic of the delay cell is in Fig. 4(a). The delay cell is voltage controlled by feeding the regulated or the reference voltage to V_C node. Both delay lines are triggered by a ring oscillator forming from the reference delay path. The

TABLE I
STATES OF Q1/Q2 CORRESPONDING TO V_{CMP}.

V_{CMP} States	Q1	Q2
V_{CMP} <0.495V	1	1
0.495V <V_{CMP} <0.505V	0	1
0.505V <V_{CMP}	0	0



(a) (b)

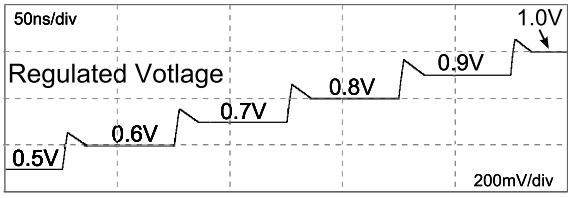
Fig. 4. Schematics of (a) the voltage controlled delay cell, and (b) the voltage divider.

period of the internal ring oscillator is 300ps. It makes sure that both delay paths are synchronized. An "enable" signal is also designed to activate or deactivate the DED.

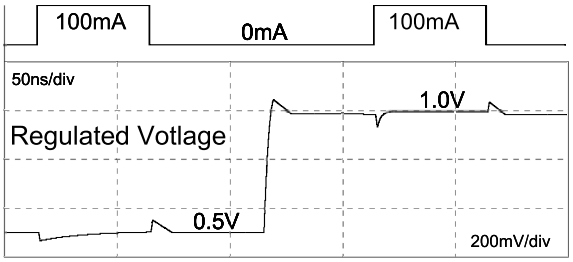
The delay cell is designed to work around V_{REF} which is 0.5V. Therefore, a voltage divider is necessary to divide the each desired regulated voltage to 0.5V. Fig. 4(b) depicts the resistive voltage divider. It takes V_{REG} as input and provides five divided voltages with different dividing ratios. Together with non-divided V_{REG}, there are six voltage outputs. Only one at a time will be passed to V_{CMP} output by the switch. For example, when demanding a 0.8V regulated voltage, the mode control block in Fig. 2 will activate the fourth switch. A 5/8 ratio will divide 0.8V to 0.5V that is able to be compared with V_{REF}.

The divided output V_{CMP} is compared with V_{REF} by the DED. If two voltages are equal, two delay lines should have equal delay. The two flipflop outputs, Q1 and Q2, will capture opposite values. When V_{CMP} is lower than V_{REF}, delay line driven by V_{CMP} will be faster. Therefore, Q1 and Q2 will both capture logic "1" values. Logic "0" values will be captured in both Q1 and Q2 when V_{CMP} is higher than V_{REF}. This condition will hold within $\pm$5mV deviation of V_{CMP} as a result of the resolution of delay lines and flipflops, The corresponding states of V_{CMP}, Q1, and Q2 are listed in Table I.

The simulation of the proposed digital controlled voltage regulator uses UMC 65nm standard CMOS technology. Only normal threshold voltage devices are used. The input supply voltage is 1.1V with a 1.5nF decoupling capacitor. Output mode changing is shown in Fig. 5(a). The overshoot when changing modes is about 50mV for all output states. The minimum error in stable state is 6mV at 0.5V output whereas maximum error is 12mV at 1V output. The error comes from the resolution of DED. Larger error of 1V output is resulted



(a)



(b)

Fig. 5. Simulated waveforms of (a) output modes, and (b) step response at full load current.

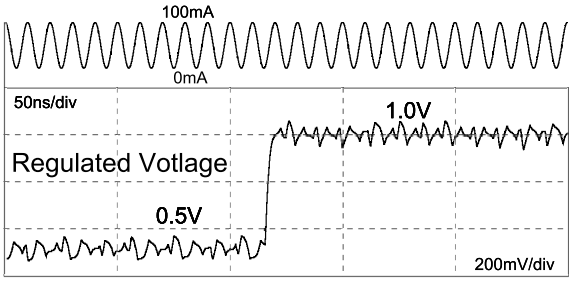


Fig. 6. Simulated waveforms of the regulated voltage under 100MHz sinusoidal load current.

from the voltage divider as well as the voltage averaging effect on the delay line. The system consumes an instant maximum of 480μA as an nature of digital implementation. But in average, the quiescent current is 128μA.

The simulated step response of the regulated voltage is shown in Fig. 5(b). For simplicity, only the step responses of 0.5V and 1V output are presented. Note that from the figure the mode changing takes about 12ns to charge from 0.5V to a stable 1V. The rise and fall time of the load current is 100ps. The maximum ripples when load current changes are 41mV and 66mV for 0.5V and 1V output, respectively. Again the ripple of 1V output is larger than that of 0.5V output.

III. Time Interleaving Control

The discrete operation of the digital circuits is a challenge for the digital control loop compared to the continuous operation of analog circuits. If the load current changes as time instead of a steady value, e.g. a 100MHz sinusoidal current load, the output will ripple and the magnitude will be worsened as shown in Fig. 6. The output ripples become 55mV and 80mV for 0.5V and 1V output, respectively. In order to improve the control loop response, a time interleaving control is proposed.

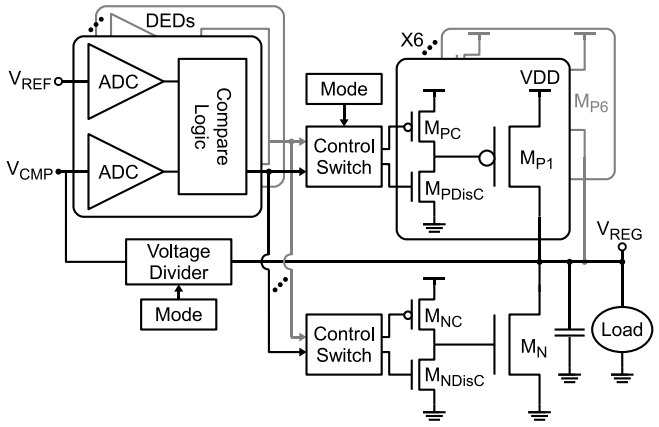


Fig. 7. Block diagram of proposed time interleaving digital controlled linear regulator.

TABLE II
Performance Comparison of Time Interleaving Control

Control Type	Quiescent Current (μA)	Maximum Ripple (mV)			
		Step Response		100MHz Sin. Load	
		0.5V	1V	0.5V	1V
Single	128	41(8.2%)	66(6.6%)	55(11%)	80(8%)
Dual	366	34(6.8%)	56(5.6%)	51(10.2%)	62(6.2%)
Triple	546	41(8.2%)	51(5.1%)	47(9.4%)	64(6.4%)

The idea is to make copies of DED block as Fig. 7 depicts. The control system interleaved uses the results of different DEDs to control the output device. The duplicated DED is also triggered by the ring oscillator from the reference delay path of the first DED with a certain delay. The delay is designed to equally divide the 300ps period. If two DEDs are used, the delay of the trigger signal is 150ps for the second DED. For three duplications case, the delay are 100ps and 200ps for the second and the third DEDs, respectively. The control switch is required to switch between the outputs of each DED to interleaved control the output devices. By using the time interleaving control technique, the control system is enhanced from responding every 300ps to every 150ps or 100ps.

The simulated results of the time interleaving control are listed in Table II. The percentage numbers are defined by the ratio of ripple to output voltage. Except the duplicated DEDs, the added control switches also draw extra quiescent current. Therefore, dual and triple control types have larger quiescent current numbers. The output ripple performance is better for the dual control compared to the single control in either step or sinusoidal load current case. Compared to dual control type, the performance enhancement of the triple control type is not that significant. The output ripple is even larger in some cases. But the improvement compared to the single control type is still observable. Overall, the proposed time interleaving control indeed improves the performance of the discrete digital control system.

TABLE III
PERFORMANCE COMPARISON OF VOLTAGE REGULATORS

	[3] 2004	[7] 2007	[5] 2008	[6] 2009	This work
Technology	90nm	90nm	0.35μm	0.13μm	65nm
V_{IN}	1.2V	2.4V	3.5V	1.15V	1.1V
V_{OUT}	0.9V	1.2V	0.9V	1V	0.5-1V
I_{OUT}	100mA	1A	50mA	25mA	100mA
ΔV_{OUT}	90mV	120mV	6.6mV	15mV	80mV
I_Q	6mA	25.7mA	164μA	50μA	128μA
C_{decap}	0.6nF	2.4nF	1μF	4μF	1.5nF
Current Efficiency	94.3%	97.5%	99.7%	99.8%	99.9%
T_R [7]	540ps	288ps	132ns	2.4μs	1.2ns
FOM [7]	32ps	7.4ps	433ps	4.8ns	1.54ps
Implementation	analog	digital	analog	analog	digital

IV. DISCUSSIONS

The simulation results presented in this paper are all done with UMC 65nm standard CMOS technology. Unlike the analog voltage regulator that suffers from advanced technology, digital implementation instead benefits from advanced technology. If implementing the same delay cell as Fig. 4(a) in 90nm technology, the period of the ring oscillator will be almost 700ps. It is more than twice of the single control type response time of 300ps. Moreover, the delay changes corresponding to the control voltage variations are smaller in 90nm technology. The delay line is required to be longer to have the same sensitivity to the voltage. Longer delay line draws more current itself. The increased response time requires more copies of DED block to achieve a performance comparable to that of 65nm technology. The duplication incurs more power. Therefore, digital style voltage regulator benefits from more advanced technology in either aspect of power or response speed.

As the results presented in Sec. III suggest, there is a tradeoff between the quiescent current and the output ripple performance. Making one extra copy of DED block results in more than doubling the quiescent current of single control type. But the output ripple does reduce with more time interleaving control blocks. The simulation results listed in Table II show that with dual control type, the quiescent current increment is acceptable with observable ripple reduction. However, adding the third control blocks further increases the quiescent current without having significant performance improvement. Therefore, dual type time interleaving control will be a good choice in this work.

In Table III, the proposed digital controlled voltage regulator is compared with publications in literature. Two of these previous works aimed for integration with small decoupling capacitor [3], [7] whereas the other two aimed for minimum output ripple [5], [6] using large offchip capacitors. The quiescent current of the proposed work is much lower than [3] and [7] and is comparable with [5] and [6]. The 99.9% current efficiency is the highest among these works. Different regulators can be compared on the basis of following figure of merit [7]

$$FOM = T_R \times \frac{I_Q}{I_{OUT}} = \frac{C_{decap} \times \Delta V_{OUT}}{I_{OUT}} \times \frac{I_Q}{I_{OUT}}. \quad (1)$$

The proposed regulator achieves the lowest and the best FOM which is 1.54ps for single control type. This is contributed mainly by the low quiescent current and high current efficiency of the digital control system.

V. CONCLUSION

A fully digital controlled push-pull linear voltage regulator is presented in this paper. All the simulations use UMC 65nm standard CMOS technology. The regulated output voltage is variable ranging from 0.5V to 1V in steps of 0.1V. The designed regulator is capable of supplying 100mA load current for every output level. The output devices are grouped and activated separately at different output level to reduce the power consumption. A time interleaving control technique is also presented to enhance the output performance. The ripple of the output voltage when the load or output level changes is smaller than 10% of that specific output level. The quiescent current is only 126μA and the current efficiency is 99.9% high. Therefore, the presented work in this paper achieves the best speed-power figure of merit among the previous works in literature.

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