Near-/Sub-V_{th} Process, Voltage, and Temperature (PVT) Sensors with Dynamic Voltage Selection

Ming-Hung Chang[1], Shang-Yuan Lin[1], Pei-Chen Wu[1], Olesya Zakoretska[1], Ching-Te Chuang[1], Kuan-Neng Chen[1], Chen-Chao Wang[2], Kua-Hua Chen[2], Chi-Tsung Chiu[2], Ho-Ming Tong[2], and Wei Hwang[1,2]
Department of Electronics Engineering & Institute of Electronics[1], National Chiao Tung University, Hsinchu, Taiwan
Advanced Semiconductor Engineering (ASE) Group[2], Kaohsiung, Taiwan

***Abstract*—A process, voltage and temperature (PVT) sensors with dynamic voltage selection are proposed for environmental management in the ultra-low voltage dynamic voltage and frequency scaling (DVFS) system. The process and voltage (PV) sensors initially monitor the process variation. With known process information, PV sensors can real-time provide voltage variation status. The temperature sensor has six temperature sensitive ring oscillators (TSROs) generating frequency proportional to temperature. It dynamically selects the proper TSRO to convert the frequency into digital readings according to voltage status provided by PV sensors. With known process and voltage information from PV sensors, a pure temperature measurement result can be obtained. The proposed PVT sensors are designed in TSMC 65nm CMOS technology. This work can be dynamically operated over an ultra-low voltage range from 0.25V to 0.5V. Only 2.3µW is consumed at 0.25V. They can achieve 0.15˚C resolution and 50k samples/sec conversion rate.**

Keywords- Process, voltage, temperature (PVT) variations; temperature sensor;near-threshold circuit; sub-threshold circuit.

I. INTRODUCTION

Battery size of emerging energy-constrained applications like wearable medical devices and handheld electronics is form-factor limited or even battery-free. Lowering the supply voltage is one attractive way to gain minimum energy operation [1]. As we continue scaling down the supply voltage that the transistors reach the near/sub-threshold regions, circuits become more sensitive to process, voltage and temperature (PVT) variations than super threshold ones. The environmental variations are so large that variation-aware technique [2] is necessary to prevent functional failure. Meanwhile, process variation is getting much worse as technology aggressively scaling down. An ultra-low-voltage real-time on-chip environment sensor is the key to providing information for energy efficiency enhancement.

For energy-limited miniature devices, dynamic voltage and frequency scaling (DVFS) [3] platform with energy harvesting technique as shown in Figure 1 can achieve maximum energy saving in response to varying performance requirement. The supply voltage range provided by energy harvesting power source, e.g. solar, RF, and thermo, is near or below MOSFET threshold voltage. Several successful designs have been presented that smart temperature sensors can be accurate and low power. In [4], the PNP-based sensor achieved ±0.2˚C inaccuracy from -30˚C to 125˚C. It had a minimum power dissipation of 7.4µW. For time-domain design, a resolution of better than 0.1˚C sensor was presented in [5]. Their conversion rate were less than 10 samples/sec. One fast conversion rate of

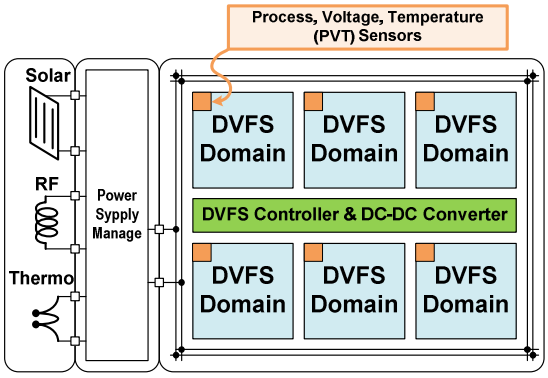

Figure 1. The ultra-low voltage DVFS system with energy harvesting.

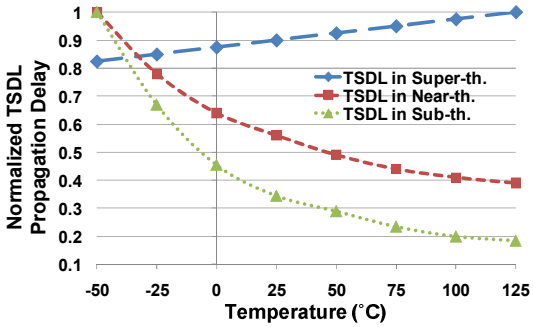

Figure 2.TSDL propagation delay in different operation region.

366k samples/sec frequency-based sensor was presented in [6]. It consumed 400µW at supply voltage 1.2V and wide temperature spread of ±2.7˚C inaccuracy. However, all of them cannot be operated in ultra-low voltage region.

Previously, we presented process, voltage, and temperature (PVT) sensors in [7]. The sensors were implemented capable of working at 0.5V to 0.3V supply voltage with a poor resolution of 0.88˚C/bit. Also, it could only been operated in a fixed supply voltage (between 0.5V to 0.3V) once the circuit calibrated. In this work, proposed PVT sensors can be operated in near-/sub-threshold region with dynamic voltage selection ability. Therefore, it can be easily applied to ultra-low voltage DVFS platform. The rest of this paper is organized as follows. Section II describes the near-/sub-threshold operation challenges for the PVT sensors. The architecture of 0.5V to 0.25V PVT sensors with dynamic voltage selection is proposed in Section III. Section IV implements individual building blocks of the proposed sensors. The simulation results of the proposed sensors under TSMC 65nm general purpose CMOS technology are shown in Section V. Finally, conclusions are given in Section VI.

II. NEAR-/SUB-THRESHOLD OPERATION CHALLENGES

A temperature-to-delay-difference generator [5] was designed to produce an output pulse with a width as linearly proportional to the measured temperature. The temperature insensitive delay line (TIDL) was inserted to avoid large DC offset. As shown in Figure 2, the characteristics of temperature sensitive delay line (TSDL) become very different as the supply voltage scaling down. The TSDL propagation delay in super-threshold region increases with temperature whereas that in sub-threshold region decreases with temperature. However, the linearity of the TSDL propagation delay in sub-threshold region is much worse. In [6], a temperature-to-frequency-difference generator was designed to have the temperature sensitive ring oscillator (TSRO) to be the clock source for up-counting, and the temperature insensitive ring oscillator (TIRO) to be the clock source for down-counting. With the same counting period, the output of the up-down counter was equal to the frequency difference of the two oscillators. However, the sensor was easily affected by environmental variations in near-/sub-threshold since it did not take process and voltage variations into considerations.

III. ARCHITECTURE

To perform dynamic thermal management of ultra-low voltage DVFS system in Figure 1, the supply voltage and process variations must be considered. The block diagram of proposed PVT sensors can be simply divided into six blocks, including finite state machine (FSM), process and voltage (PV) sensors, temperature sensor, process register, voltage mapping table, and PV compensation as shown in Figure 3. The dynamic voltage selection range is from 0.5V to 0.25V, so a voltage sensor is utilized to monitor voltage variation and provide real-time voltage information to temperature sensor. Because process variation is extremely significant in the ultra-low voltage, a process sensor is necessary as well. They are implemented as PV sensors. The FSM sends *EN_ZTC* and *EN_TSRO* to enable PV sensors and temperature sensor respectively. The PV sensors measure process and voltage information and send it to process register and voltage mapping table. According to signal of process register, *P[4:0]*, the voltage mapping table decides the present supply voltage status and send *V[2:0]* to temperature sensor. The temperature sensor performs temperature measurement by selecting supply voltage dynamically and generate temperature information, *T[11:0]*, to PV compensation block. The PV compensation block compensate *T[11:0]* with *P[4:0]* and *V[2:0]* to remove voltage and process variations induced errors.

IV. CIRCUITS IMPLEMENTATION

A. Finite State Machine

The state diagram and signal timing waveform of FSM is shown in Figure 4 and Figure 5 respectively. In the beginning, the *RESET* signal is pulled up, FSM is initialized. Later, when *RESET* signal is set to low level the sensor start sensing process condition for one CLK cycle time. After sensing process condition, *P_done* signal is pulled up to alert the process register to store the process value. Then, the sensor is idle until

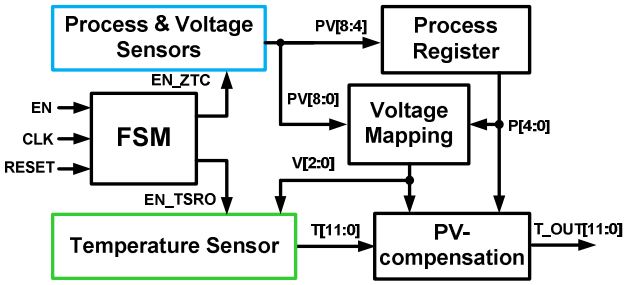

Figure 3. Architecture of proposed PVT sensors.

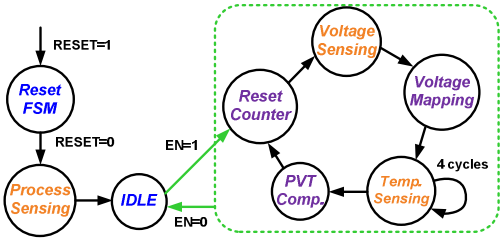

Figure 4. State diagram of FSM.

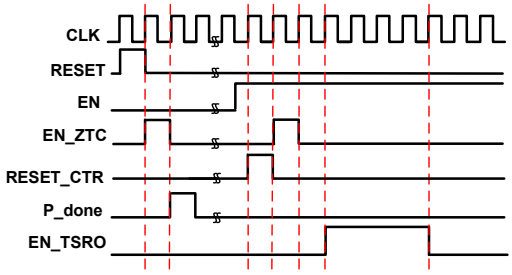

Figure 5. Signal waveform diagram of FSM.

EN signal is alerted to monitor voltage and temperature. At the first cycle, the FSM reset counters of PV sensors and temperature sensor by the reset signal *RESET_CTR*. Then, the PV sensor is enabled by *EN_ZTC* to sense voltage condition at the second cycle. Next, voltage mapping table decide current voltage range according to voltage condition sensed in the previous cycle and value in the process register. After knowing current voltage is within which range, the temperature sensor measure temperature for four cycles. Finally, PV compensation block calculates the temperature value according to value in the process register and voltage information. If *EN* is still high, FSM would back to first state. Otherwise, FSM will back to idle state.

B. PV Sensors, Process Register, and Voltage Mapping

The p-type and n-type transistors vary with temperature, process, and voltage. Mutual compensation of mobility and threshold voltage temperature variations may result in a zero temperature coefficient (ZTC) bias point of them. In TSMC 65nm bulk CMOS technology, the ZTC points of NMOS and PMOS are at about 0.4V and 0.6V respectively. According to simulation results, the delay of unit inverter will not change with temperature variation at 0.5V. The PMOS and NMOS mutual current compensation leads to the output frequency of ring oscillator is constant with temperature variation.

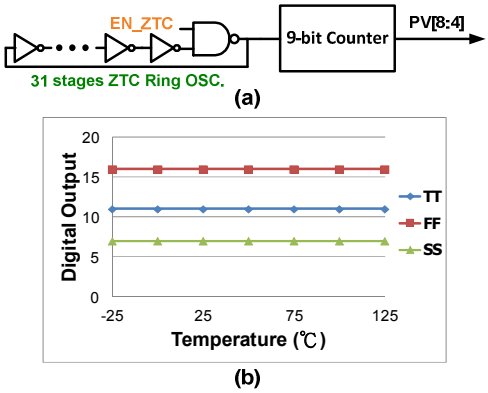

Figure 6. (a) Implement circuit of PV sensor. (b) The relationship between digital output and process variation.

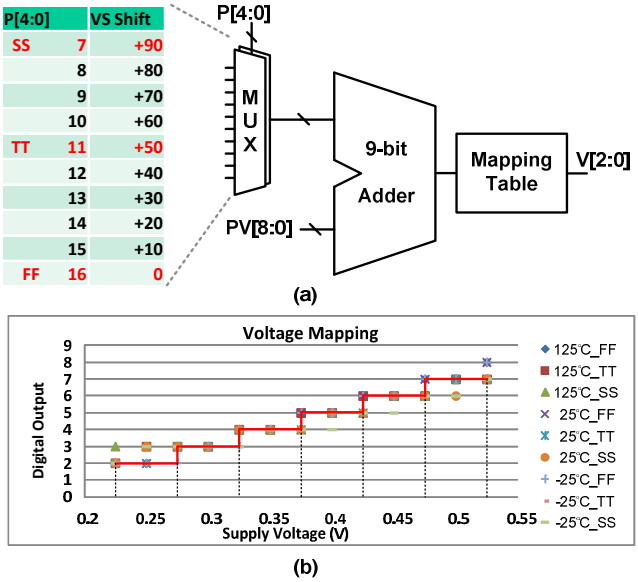

Figure 7. (a) Compensation circuits and mapping table of voltage sensor. (b) Digital output after process compensation.

The ZTC ring oscillator is the major component of PV sensors, as shown in Figure 6(a). The low threshold voltage (LVT) CMOS is adopted to construct the inverters and NAND gate. When the FSM enters to process or voltage sensing state, the *EN_ZTC* signal enable the 31 stages ZTC ring oscillator and the 9-bit counter triggered by ZTC ring oscillator. Therefore, the digital output of counter is also temperature invariant and only affected by process variation. In this work, process digital output resolution only requires *PV[8:4]* for corner measurement. When process corner is located at SS, TT and FF, the digital output is 7, 11 and 16 respectively, and is not affected by temperature as shown in Figure 6(b).

Moreover, the PV sensor can be utilized to sense supply voltage condition when supply voltage is dynamic scaling. When EN_ZTC pulse period is fixed, *PV[8:0]* digital output is proportional to voltage but lightly affected by temperature. However, the PV sensors digital output is still affected by process variation. The process information *P[4:0]* stored in process register is now used to get voltage information *V[2:0]*

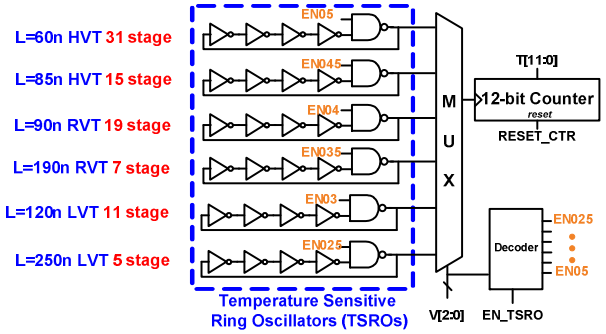

Figure 8. Implement circuit of temperature sensor.

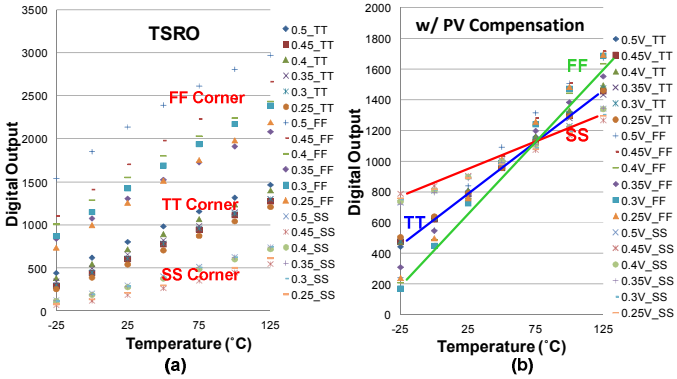

Figure 9. (a) Simulation results of temperature sensor. (b) Simulation results of compensated digital output.

from *PV[8:0]*. The block diagram of voltage mapping circuit is shown in Figure 7(a). It convert compensated value to simplified digital output, *V[2:0]*, for temperature sensor dynamic voltage selection and PV compensation. The relationship of digital output and supply voltage is shown in Figure 7(b).

C. Temperature Sensor

The temperature sensor is composed of six TSROs, a 12-bit counter, multiplexers and a decoder, as shown in Figure 8. TSROs are controlled by EN05, EN045, EN04, EN035, EN03 and EN025 and only operated when EN_TSRO is high. After voltage mapping signal, *V[2:0]*, is sent to decoder and multiplexer for dynamically selecting suitable TSRO. To ensure it matches supply voltage, dynamic voltage selection technique is achieved. The proposed temperature sensor can be operated in ultra-low voltage DVFS platform correctly.

It is noted that the threshold voltage of TSRO must equal to supply voltage at the maximum temperature operation range. Therefore, TSROs with different threshold voltage are designed for corresponding voltage between 0.25V to 0.5V. The threshold voltage behavior can be adjusted by using multi-threshold CMOS and increasing the effective channel length. Besides, the stage number of each TSRO is arranged to make digital output slope ratio be the same for resolution improvement. The simulation results of temperature sensor can be roughly separated into 3 parts, FF, TT and SS corner, as shown in Figure 9(a). For each corner, slope of different TSROs is roughly identical for convenience of compensation.

Table I. Temperature sensors comparisons

Sensor	Technology	Sensor Type	Supply(V)	Power	Conv. Rate	Resolution	Inaccuracy	Temp. Range	PV Status
[4]	0.7µm	BJT	2.5-5.5	62.5µW	10 S/sec	0.025˚C	±0.25˚C (3σ)	-70˚C ~130˚C	N
[5]	0.35µm	Delay	3.3	36.7µW	2 S/sec	0.092˚C	-0.25˚C ~0.35˚C	0˚C ~90˚C	N
[6]	65nm	Frequency	1.2	400µW	366 kS/sec	0.043˚C	-2.9˚C ~2.75˚C	-40˚C ~110˚C	N
[7]	65nm	Frequency	0.3-0.5	3.7µW	10 kS/sec	0.880˚C	-0.8˚C ~0.8˚C	-50˚C ~125˚C	Y
This Work	**65nm**	**Frequency**	**0.25-0.5**	**2.3µW**	**50 kS/sec**	**0.150˚C**	**-1.75˚C ~1.96˚C**	**-25˚C ~125˚C**	**Y**

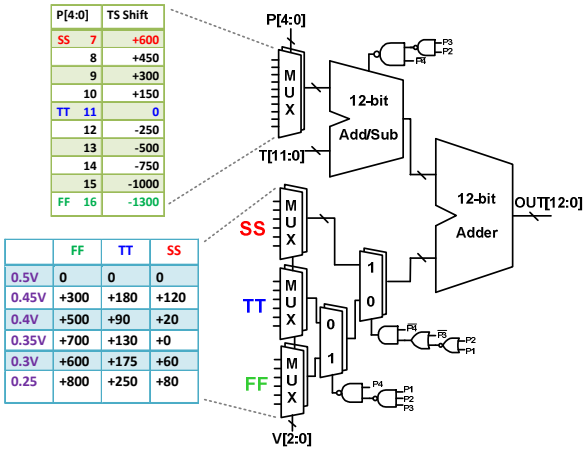

Figure 10. PV-compensation circuits and compensation value tables.

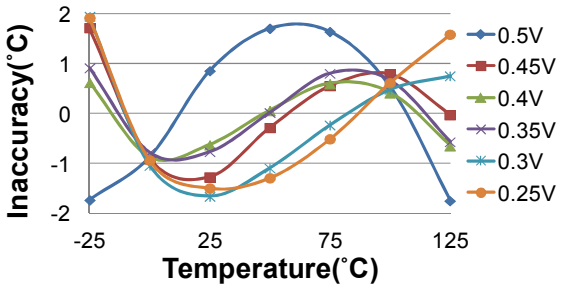

Figure 11.Simulation error of proposed temperature sensor.

D. PV Compensation

When proposed FSM enters to PV compensation state, digital output of temperature sensor is compensated according to *P[4:0]* stored in process register and *V[2:0]* sent from voltage mapping table as shown in Figure 10. The 12-bit adder and substrator are utilized to calculate temperature digital output. The multiplexers will choose appropriate compensating value based on current process and voltage information. The final results of compensated digital output are shown in the Figure 9(b). The proposed temperature sensor can generate digital output free of process and voltage variations in ultra-low voltage.

V. Simulation Results

The proposed process, voltage and temperature sensors are implemented under TSMC general purpose 65-nm CMOS technology. The supply voltage can be scaled from 0.25V to 0.5V. The temperature simulation error is -1.76˚C to 1.96˚C in the range of -25˚C to 125˚C as shown in Figure 11. The effective resolution is 0.15˚C/LSB at 50k samples/sec conversion rate. The minimum power consumption is about 2.3µW at 0.25V supply voltage. In Table I, the achieved performance of proposed ultra-low process, voltage, and temperature sensors are compared with recent temperature sensors [4]-[7]. The proposed temperature sensor has dynamic voltage selection ability, high conversion rate and ultra-low power consumption. The temperature inaccuracy of proposed temperature sensor is sufficient for dynamic thermal management applications.

VI. Conclusion

The frequency-based process, voltage and temperature sensors are proposed for on-chip temperature measurement in the ultra-low voltage DVFS systems of energy harvesting. It composed of process, voltage and temperature sensors. The process sensor and voltage (PV) sensors monitor the process variation and voltage variation continuously and give the variation information for temperature compensation. The temperature sensor has six TSROs generating frequency proportional to the measurement temperature at suitable supply voltage, and converts the frequency into digital code. The PVT sensors are designed in TSMC 65nm CMOS technology. It can operate over an ultra-low supply voltage range from 0.25V to 0.5V. The power consumption is 2.3µW at 0.25V supply voltage and 50k samples/sec conversion rate. The above characteristics make the proposed PVT sensors suitable for energy-harvesting miniature portable platform.

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