Near-/Sub-threshold DLL-based Clock Generator with PVT-aware Locking Range Compensation

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***Abstract*—A near-/sub-threshold programmable clock generator is proposed in this paper. The major challenge of the ultra-low voltage (ULV) circuits is that the lock-in range of the delay line is easily affected by the environmental variations. In the proposed clock generator, there is a PVT compensation unit which consists of a set of delay line and a PVT detector. The unit is responsible for adjusting the lock-in range of clock generator to guarantee successful clock lock. In addition, the variation-aware logic design is performed in the clock generator, which improves the reliability on process variation. Also, the adoption of pulse-circulating scheme suppresses process induced output clock jitter. Furthermore, it has the ability to generate the output clock with frequency from 1/8 to 4 times of the reference clock. The clock generator has been designed using UMC 65nm CMOS technology. The frequencies of reference clock are 625 kHz at 0.2V and 5MHz at 0.5V. The power consumptions are 0.18µW and 5.17µW, respectively, at 0.2V and 0.5V. The core area of this clock generator is 0.01mm^2.**

Keywords-delay-locked loop; near-/sub-threshold circuits; PVT-aware design

I. INTRODUCTION

With the evolution of CMOS process technology, the number of transistors in a digital core doubles about every two years. The increases of transistor density and operating frequency have brought the effect of shorter battery life. For some applications such as wireless body area network (WBAN) sensors, the critical consideration is life time instead of operating frequency. The WBAN system provides body signal collecting and reliable physical monitoring. It has many wireless sensor nodes (WANs) attached on or implanted inside human body. How to perform a ULV design and simultaneously conform to the performance and reliability requirements is an important issue. Even though degradation in speed and increased susceptibility to parameter variations, the power dissipation can be achieved by operating digital circuits with scaled supply voltages. The operating voltage is scaled down to near-threshold (0.5V) or sub-threshold (0.2V) region depending on the power and speed requirements of the target systems.

Dynamic-voltage-and-frequency-scaling (DVFS) technique is widely used to achieve the goal of saving powers. Besides, advances in ULV circuit design have demonstrated capabilities to reduce the power consumptions. The mix of DVFS and ULV design techniques has a great potential for the ultra-low power demands. In the DVFS system, the clock generation and transmission are realized by clock generator and clock tree. The mainly possible problems in clock system are clock jitter and skew. Jitter comes from clock generator, and skew comes from clock tree. They may cause functional errors in digital circuits, and will be more serious in ULV region because of environmental variations. The environmental variations include process, voltage, and temperature (PVT); they should be considered carefully when designing ULV circuits.

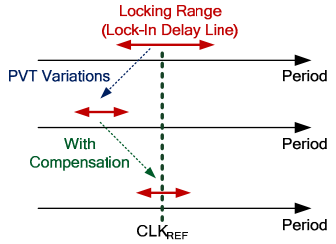

Figure 1. Concept diagram of PVT compensation.

In near-/sub-threshold operations, the device behaviors are affected more seriously by PVT variations than that in the super-threshold region. For the clock generator, the influenced devices make the lock-in delay line having different delay range. Therefore, the clock generator probably cannot be locked to reference clock. Fig. 1 shows the concept diagram of PVT compensation. In the typical condition, the reference clock is in the locking range of lock-in delay line. When there are PVT variations, the locking range is shifted. The clock generator cannot be locked to reference clock. After adding the PVT compensation, the locking range can be adjusted. Additionally, the variation-aware logic design is performed for near-/sub-threshold operation.

Many clock multiplication schemes have been proposed for DVFS systems in super-threshold region. Phase-locked loops (PLLs) are usually used as clock generators, but its locking period takes hundred of reference clock cycles. To enhance the flexibility of clock generator for DVFS system, an all-digital clock generator was presented [1] to produce output clock by delaying the reference clock dynamically based on the frequency control code. However, delay-locked loop (DLL) was presented for DVFS system, it could not generate

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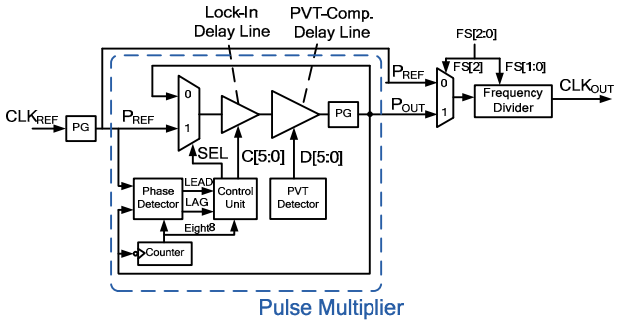


Figure 2. Proposed clock generator for near-/sub-threshold DVFS system.

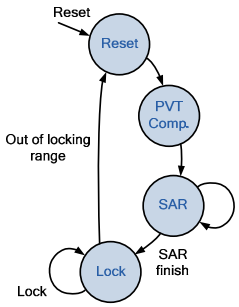


Figure 3. Proposed finite state machine (FSM).

fractional clock. Cyclic clock multiplier (CCM) has been presented for DVFS applications, and it has the advantage of creating fractional or multiplied clock. However, the cyclic clock multiplier with time-to-digital converters (TDC) for phase error detection occupied large area and consumed more power. A programmable clock generator is proposed in this paper to achieve reliable operation in near-/sub-threshold region. It adopts the pulse-circulating scheme in [2]. The proposed clock generator can produce multiplier and fractional clock without the area overhead. Comparing with DLLs based on clock multiplier, the process-induced phase error can be reduced since the pulse always circulates through the same delay line.

This paper is organized as follows. Section II describes the system architecture of the proposed clock generator. The PVT compensation technique and the implementation of circuits are discussed in Section III and Section IV, respectively. The simulation results are given in Section V. Finally, Section VI concludes this work.

II. System Architecture

The architecture of the proposed clock generator is shown in Fig. 2. The main blocks of the clock generator are pulse generators (PG), phase detector, counter, lock-in delay line, PVT compensation (PVT-comp.) delay line, PVT detector, control unit and frequency divider.

In the proposed clock generator, the CLK_{REF} signal enters a PG which produces pulse (P_{REF}) with frequency equal to CLK_{REF}. Pulse multiplier generates pulses (P_{OUT}) with 8-time frequency of the reference pulse (P_{REF}). The divider can divide the input frequency by 2, 4, 6 or 8. Therefore, the proposed clock generator is able to output clock with M/N times of the reference clock, M=(1,8) and N=(2,4,6,8) which are controlled

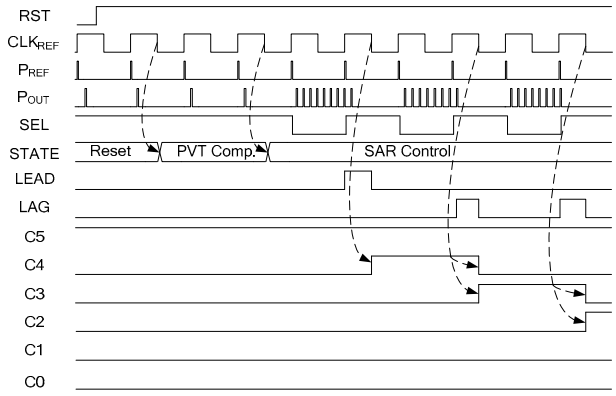


Figure 4. Timing diagram of the proposed FSM operating from Reset to SAR state.

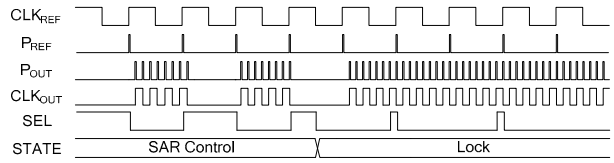


Figure 5. Timing diagram of the proposed FSM operating from SAR to Lock state.

by input frequency selecting signal *FS[2:0]*. The frequency selection range is from 0.125X to 4X with eight different multiplied output frequencies.

In order to produce P_{OUT} with 8-time frequency of P_{REF}, a pulse-circulating scheme is adopted. Each pulse of P_{REF} enters the circulating path and circulates 8 times. The path is determined by path selection signal *SEL*. When *SEL*=1 the pulse from P_{REF} can enter the delay line. Otherwise, the circulating path is built. The counter is used to count the number of times that pulse flows in the pulse-circulating path. It informs phase detector and control block by the signal *Eight8* when it is equal to eight. Therefore, the phase detector compares the phases of P_{OUT} and P_{REF} when the counting number is equal to eight.

Fig. 3 demonstrates the procedure of proposed clock generator operation. After the clock generator is reset, the finite state machine passes through three steps: PVT compensation, SAR (successive approximation register) control, and lock. In the first step, the system goes into the PVT compensation state. To compensate the locking range for the delay variations, the clock generator uses the PVT compensation technique to provide adequate delay for the lock-in delay line. In this step, the locking range of the two delay lines are modified to ensure the period of the reference clock within the locking range. After PVT compensation, the FSM enters the second step, SAR control. It adopts binary search algorithm to trace the reference clock. In the step, the control unit changes the control codes (*C[5:0]*) according to the comparison results of the phase detector (*LEAD* and *LAG*). The total delay of lock-in delay line and PVT-comp. delay line is tuned to be equal to the period of the reference clock. It also means the pulse multiplier is locked. Finally, the FSM enters lock state, and the clock generator can output clock with multiplied or divided frequency. The feedback loop consists of output clock, phase detector, and

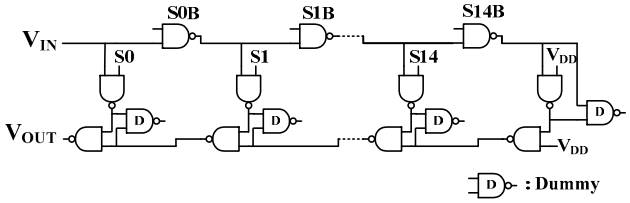


Figure 6. Topology of delay line (lattice delay line [4]) used in the proposed clock generator.

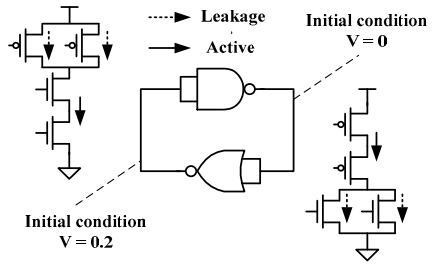


Figure 7. Back-to-back configuration.

control unit. Because SAR algorithm has an open loop characteristic which means it cannot track the environmental variations, we used another strategy to make the system in a closed loop when the SAR control finished. That is, the control unit continues the tracking procedure by adding or subtracting *C[5:0]* by 1 at a time because keeping the circuit in close loop guarantees the clock generator is still locked to reference clock.

Fig. 4 and Fig. 5 show the timing diagram of the proposed FSM operating from Reset to Lock state. The control codes *C[5:0]* change every two clock cycles. Fig. 4 also shows that the proposed clock generator has the ability of the PVT compensation for the range of the lock-in delay line and takes only two reference clock cycles.

III. PVT-AWARE DELAY LINE DESIGN

A. Variation-Aware Lock-in Delay Line

The lock-in delay line (LIDL) is modified from the nested lattice delay line (NLDL) [4], as Fig. 6 shown. Compared with the NLDL, the LIDL saves some circuit area by using the 14-stage FO2-NAND instead of the lattice delay line (LDL) as a block delay. It still keeps the advantages of the NLDL. First, the LIDL has equal rising and falling times. Second, while the tuning range increases, the maximum operating frequency will be the same. Finally, the variation is only half compared to conventional configuration. The locking range of the lock-in delay line is from $4\times D_{NAND,FO2}$ to $130\times D_{NAND,FO2}$. Initially, the lock-in delay line is set to be about the middle point of locking range, $64\times D_{NAND,FO2}$.

When the supply voltage is down to sub-threshold region, there are two critical factors affect functionality [5]. First, the ratio of I_{ON} to I_{OFF} is decreased in logic gates. Second, random-dopant-fluctuation is a source of local variations in sub-threshold region [6]. These two factors result in not only reduced output swings in CMOS logic gates but also skewed voltage transfer curve (VTC). Upsizing transistor is one technique for mitigating local variation. Researches in [7] showed that standard deviation of V_t varies inversely with the square root of

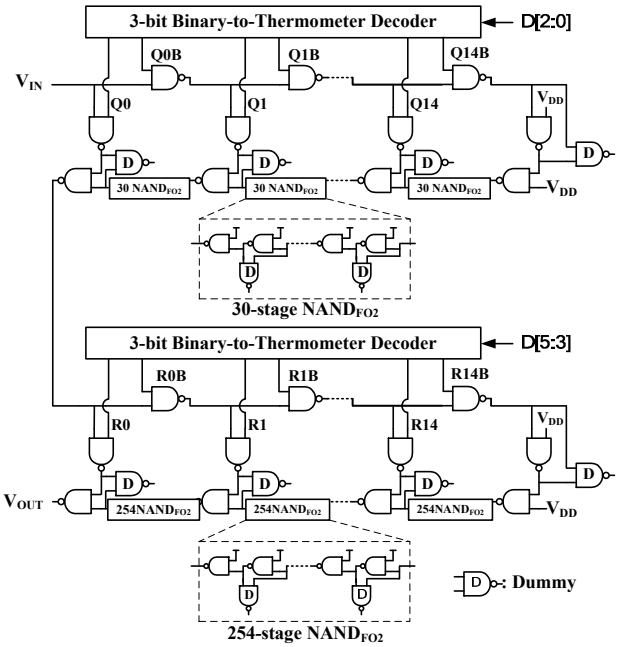


Figure 8. PVT compensation delay line.

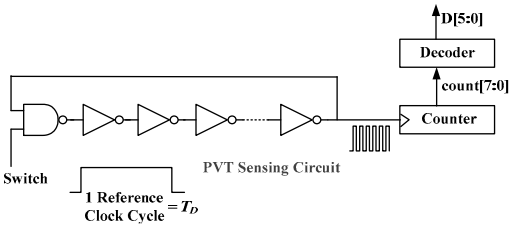


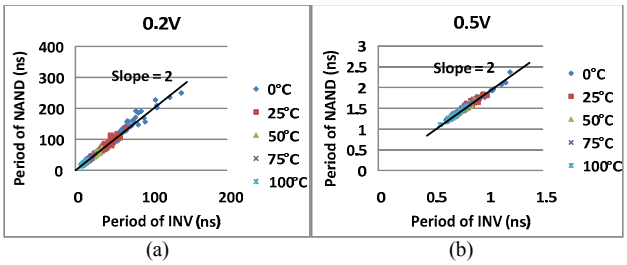
Figure 9. PVT detector.

the channel area. In the proposed clock, we use the back-to-back configuration [5] to find the length and width of the transistors and to make sure the function work correctly as Fig. 7 shown.

B. PVT Compensation Delay Line

Fig. 8 shows the PVT compensation (PVT-comp.) delay line, it is also similar to the nested lattice delay line (NLDL). Fig. 2 shows that the PVT-comp. delay line is controlled by *D[5:0]*. In the PVT compensation state, the PVT detector senses the environmental conditions, which are recorded in a counted number *count*. Then *count* is decoded to control code *D[5:0]*, the PVT-comp. delay line can provide adequate delay. The PVT detector is shown in Fig. 9. It consists of a PVT sensing circuit, a counter and a decoder. The PVT sensing circuit uses a ring oscillator which can be switched on or off. When the clock generator is in PVT compensation state, the switch signal is turned on for one reference clock cycle.

The ring oscillator of the PVT sensing circuit is composed of 62-stage FO1-INV and 1-stage NAND. According to the Monte Carlo simulation results, the period of the ring oscillator's output is nearly equal to the 128-stage FO1-INV delay, $128\times D_{INV}$. Thus, the counted number *count* is equal to



(a) (b)

Figure 10. Monte Carlo simulations for periods of ring oscillators (composed of FO1-INV and FO2-NAND) (a) at 0.2V, (b) at 0.5V.

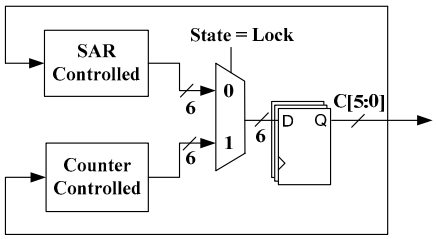


Figure 11. Lock-in delay line controller.

$$count = \frac{T_D}{128 \times D_{INV}}. \quad (1)$$

where T_D represents one reference clock cycle.

The delay period relationship between FO1-INV and FO2-NAND is expressed in (2), and it defines the relationship we adopted in subsection III.C

$$D_{NAND,FO2} = 2 \times D_{INV}. \quad (2)$$

$D_{NAND,FO2}$ represents delay of FO2-NAND. Equation (1) becomes

$$count = \frac{T_D}{64 \times D_{NAND,FO2}}. \quad (3)$$

The pulse signal propagates through the delay line eight times because the clock generator adopts the pulse-circulating scheme with the output pulses of 8 times frequency. For locking to the reference clock, the target delay of both delay lines should be equal to $T_D/8$. Equation (3) becomes

$$\frac{T_D}{8} = count \times 8 \times D_{NAND,FO2}$$
$$= (count \times 8 - 64) \times D_{NAND,FO2} + 64 \times D_{NAND,FO2}. \quad (4)$$

The delay of entire delay line is divided into two parts: the delays provided by PVT comp. delay line and by lock-in delay line. The initial delay of the lock-in delay line is set at $64 \times D_{NAND,FO2}$. From (4), the remaining delay is compensated by PVT comp. delay line. The unit delay step of the PVT-comp. delay line is $32 \times D_{NAND,FO2}$. To calculate control codes *D[5:0]*, we divide the delay provided by PVT-comp. delay line in (4) by $32 \times D_{NAND,FO2}$

$$D[5:0] = \frac{1}{32 \times D_{NAND,FO2}} \left[(count \times 8 - 64) \times D_{NAND,FO2} \right]$$

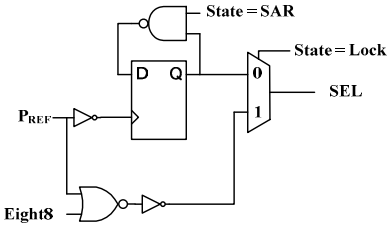


Figure 12. SEL generator.

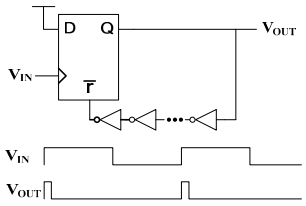


Figure 13. Pulse generator.

$$= \frac{count}{4} - 2. \quad (5)$$

Note that the minimum value of *D[5:0]* is 0 because the delay provided by PVT-comp. delay line cannot be negative. To realize the decoder to derive (5), the divisor of *count* can be accomplished with shift 2-bit to reduce area overhead.

C. Delay Ratio of FO1-INV to FO2-NAND

The delay ratio of inverter with fan-out 1 (FO1-INV) to NAND gate with fan-out 2 (FO2-NAND) is demonstrated in this subsection. The characteristic is used for PVT compensation to adjust locking range of delay line. The FO1-INV is taken as the cell of PVT sensing circuits in the PVT detector. The FO2-NAND delay is used as a unit delay step which can be tuned in the lock-in delay line, and the topology is shown in Fig. 6.

The sizes of NMOS and PMOS are the same in FO1-INV. Fig. 10 shows Monte Carlo simulation results of the oscillators at 0.2V (sub-threshold region) and 0.5V (near-threshold region). Whether the supply voltage is 0.2V or 0.5V, the delay ratios of FO2-NAND to FO1-INV both equal to 2. This ratio is unchanged under various PVT conditions. This property is used in PVT compensation delay line for locking range tuning.

IV. Circuit Description

A. Control Unit

The control unit generates the control signals, *C[5:0] and SEL*. It is composed of two parts including the lock-in delay line controller and the SEL generator. The lock-in delay line controller generates the signal *C[5:0]*, which is the lock-in delay line control codes to adjust the delay of the lock-in delay line and make the output clock close to the reference clock. The SEL generator produces the signal *SEL*, which is used to select the input clock in the pulse-circulating path according to the signal *Eight8* and the reference pulse.

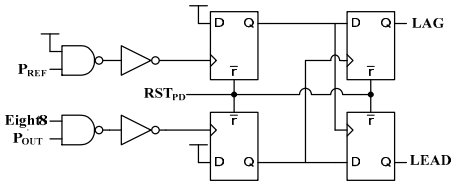


Figure 14. Phase detector.

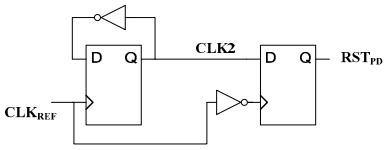


Figure 15. RSTPD generator.

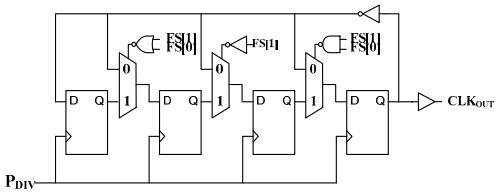


Figure 16. Frequency divider.

1) Lock-in delay line controller: The lock-in delay line controller, shown in Fig. 11, combines two categories of locking strategy: SAR (Successive Approximation Register) controlled [9] and counter controlled [10]. The SAR controlled strategy adopts binary search algorithm, which achieves short locking time and low hardware complexity. Nevertheless, its open-loop characteristic doesn't track the environmental variations. To solve this problem, the counter controlled strategy is added. It is aimed at tracking of the environmental variations for its close-loop characteristic. When the clock generator starts, it uses the SAR strategy first for fast locking. After the SAR controlled strategy finished, it is changed to the counter controlled strategy. *C[5:0]* is the lock-in delay line control codes. It is sent back to the combination logic blocks. The multiplexer chooses which lock-in strategy to be used. When the clock generator is in locked state, it chooses the counter controlled locking strategy tracking the environmental variations.

2) SEL generator: In Fig. 2, the *SEL* signal selects the path of the pulses from P_{OUT} or P_{REF}. If the pulse signal is from P_{REF}, the circulating pulses are re-adjusted. If the pulse signal is from P_{OUT}, the pulse-circulating path is built. Fig. 12 shows the block diagram of the SEL generator, it has two different modes at states SAR and Lock. When the state is SAR, *SEL* will be inversed every negative edge of P_{REF}. When the state is Lock, *SEL* is decided by P_{REF} and *Eight8*. *SEL* will be high when P_{REF} is high or 8th pulse of P_{OUT} arrives, and the latter is designed to avoid 9th pulse propagating through the pulse-circulating path early.

B. Pulse Generator

To circulate a pulse in the LIDL, the pulse width and the duty cycle should be design properly to avoid the pulse disappearing. Fig. 13 shows the pulse generator which is composed of a D flip-flop and the delay line. The pulse is generated when there is a rising edge in V_{IN}.

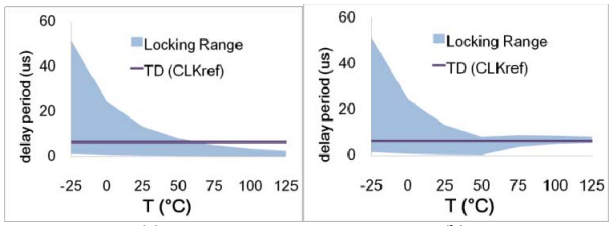


Figure 17. PVT compensation for locking range of clock generator at 0.2V TT corner (a) before compensation, (b) after compensation.

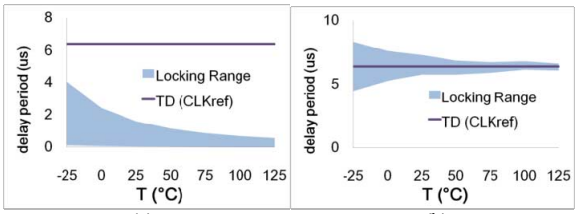


Figure 18. PVT compensation for locking range of clock generator at 0.2V FF corner (a) before compensation, (b) after compensation.

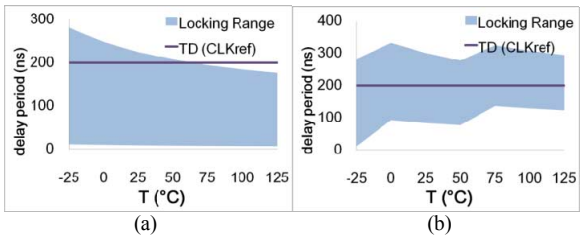


Figure 19. PVT compensation for locking range of clock generator at 0.5V TT corner (a) before compensation, (b) after compensation.

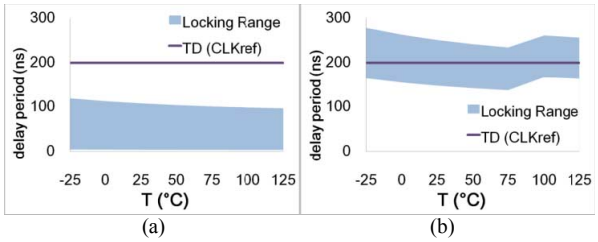


Figure 20. PVT compensation for locking range of clock generator at 0.5V FF corner (a) before compensation, (b) after compensation.

C. Phase Detector

In Fig. 14, the phase detector compares the arrival time of P_{REF} and 8th P_{OUT}. Conventional phase detector uses only two D flip-flops, which is not suitable in pulse-circulating scheme because they are easily affected by other pulse signals. Here we added another two D flip-flops in front of them. The *Eight8* signal will make the modified phase detector to work correctly. Therefore, the modified phase detector can compare only P_{REF} and the 8th pulse P_{OUT} without noised by the other pulses of P_{OUT}. In addition, we used the RST_{PD} signal, which resets the four D flip-flops, to control the modified phase detector. Fig. 15 shows the RST_{PD} generator which consists of two D flip-flops and the reference clock as the input. The phase comparison is performed every two clock cycles.

TABLE I. SUMMARY OF THE PROPOSED CLOCK GENERATOR

Near-/Sub-threshold Programmable Clock Generator	
Supply Voltage	0.2~0.5V
Process	UMC 65nm CMOS
Area	$0.077\times0.125mm^2$
Reference Clock	156kHz @ 0.2V 5MHz @ 0.5V
Maximum Output Frequency	625kHz @ 0.2V 20MHz @ 0.5V
Minimum Output Frequency	19.5kHz @ 0.2V 625kHz @ 0.5V
Output Jitter	60ns @ 625kHz CLK_{OUT}, 0.2V 4ns @ 20MHz CLK_{OUT}, 0.5V
Power Consumption	0.18µW @ 625kHz CLK_{OUT}, 0.2V 5.17µW @ 20MHz CLK_{OUT}, 0.5V

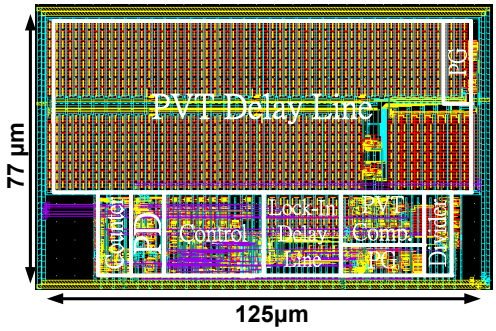


Figure 21. Layout view of the proposed clock generator.

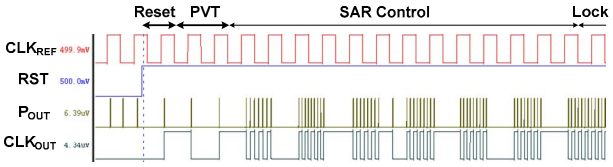


Figure 22. Post-layout simulation results at supply voltage 0.5V.

D. *Frequency Divider*

The frequency divider shown in Fig. 16 is able to divide the frequency of P_{DIV} by 2, 4, 6, or 8, according to frequency selection signal *FS[2:0]*. The number of division is decided based on how many flip-flops are in the loop. For example, when *FS[1:0]* is equal to 11, the clock loop propagate through only one flip-flop. Thus, the output frequency is the division of P_{DIV} by 2. This frequency divider is capable of producing 50% duty cycle output clock.

V. SIMULATION RESULTS

The proposed programmable clock generator for near-/sub-threshold DVFS system is implemented in UMC 65nm CMOS technology. It can operate in the voltage range from 0.2V to 0.5V. At 0.2V, the frequency of reference clock is 156kHz. It consumes 0.18µW with maximum output frequency 625kHz. At 0.5V, the frequency of reference clock is 5MHz. It consumes 5.17µW with maximum output frequency 20MHz.

Fig. 17 to Fig. 20 demonstrates the PVT compensation for the locking range of clock generator. Before compensation the reference clock is not in the locking range because of the effects of environmental variations. The clock generator is not able to output multiplied clock. After PVT compensation, the reference clock is in the locking range for various environmental conditions. Table 1 gives the performance summary of the proposed clock generator. The layout view of the proposed clock generator and the post-layout simulation results are shown in Fig. 21 and Fig. 22, respectively. The core area of this clock generator is 77µm x 125µm.

VI. CONCLUSION

A programmable clock generator was proposed for a near-/sub-threshold dynamic voltage and frequency scaling system. With the proposed PVT compensation technique, the clock generator could be protected from the PVT variations under the ultra-low voltage operations from 0.2V to 0.5V. It guarantees the reference clock is always within the locking range of the delay lines. Additionally, using the variation-aware design made the proposed clock generator more reliable. Adopting the pulse-circulating scheme improved the clock jitter performance. Besides, it can generate output frequency from 1/8 to 4 times of reference clock with eight different multiplied output frequencies. The proposed clock generator has been implemented in UMC 65nm CMOS technology. It can provide 20MHz and 625kHz at supply voltage 0.5V and 0.2V, respectively. The corresponding power consumptions are 5.17µW and 0.18µW, respectively. It is suitable to be the clock source for emerging ultra-low voltage energy-constrained applications.

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