Study of TSV Formation with ICP Parameter Control

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In this paper, a detailed research on TSV etching by inductive coupled plasma (ICP) is presented. Bosch process is used to achieve high aspect ratio etching. During TSV etching, micro-masking issue emerges when etching parameters is not optimized. Two methods have been proposed to eliminate micro-masking, including usage of isotropic recipe and parameter adjustment during etching.

1 Introduction

Development of traditional transistors has encountered a serious problem to extend Moore's Law with the physical limitation of devices. 3D IC, with many advantages such as package density improvement and power consumption reduction [1-3], is a promising solution. TSV, which connects upper and lower structure in the stacked chip, is one of the important key components in 3D IC. Therefore, TSV formation by Bosch process is crucial to decide the quality of connection in 3D IC. In this paper, two different TSV etching methods are presented. In addition, with particles from hard mask in the bottom of via, micro-masking issue is observed but can be solved by using isotropic etching or adjusting ICP internal parameters during Bosch etching.

2 Experimental

A 500 nm-thick aluminum layer was deposited as etching mask and then patterned on the wafer. Bosch process was applied for TSV deep reactive ion etching using an Oerlikon DSE ICP etcher. Bosch process includes three steps to achieve high aspect ratio of TSV. First, gas flow of SF_6 performs the Si etching. Second, gas flow of C_4F_8 deposits a polymer protection layer on the etched via to prevent sidewall etching at the following etching step. Finally, a vertical ion bombardment toward the bottom of via is applied to remove the polymer protection, which makes sure SF_6 could contact silicon to continue etching the bottom of TSV. "One loop" includes the complete three steps.

The etching principle of Oerlikon ICP reactor is based on inductive coil and inducts a strong magnetic field to increase electron moving distance for high density plasma generation.

Table 1 The Bosch process parameter for etching silicon by ICP

Parameters	Passivation	Ion Bombardment	Etching
Process Time	1 sec	1.5 sec	3 sec
SF_6 Flow	0 sccm	150 sccm	150sccm
C_4F_8 Flow	150 sccm	0 sccm	0 sccm
ICP Power	2000 w	2000 w	2000 w
Bias Power	10 w	325 w	10 w
Pressure	30 mTorr	30 mTorr	30 mTorr

3 Results and Discussion

3.1 Micro-masking removal by isotropic etching

After Bosch process, micro-masking can be observed at the bottom of TSV. The Bosch process parameters used in this experiment are shown in Table 1. In this research, the isotropic etching recipe was used to remove micro-masking. Different parameters of isotropic etching, pressure and RF bias, were studied the effects on TSV etching formation.

According to experiment results, by reducing pressure from 30 mtorr to 10 mtorr, the height of micro-masking reduces from 23 μm to 12 μm. Figs. 1 and 2 show the SEM images of TSV before and after pressure reduction, respectively. The difference comes from that lower pressure results in longer mean free path of SF_6, which let SF_6 flow deeper into via.

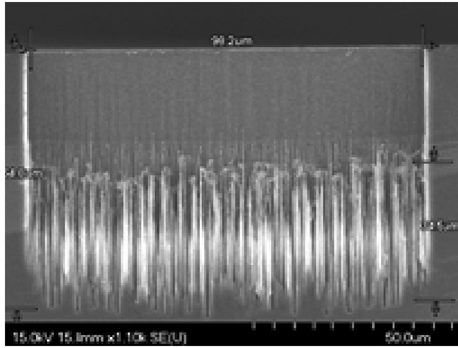

Fig. 1 The bottom of TSV before pressure reduction.

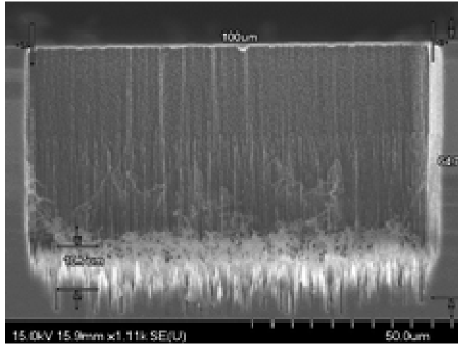

Fig. 2 The bottom of TSV after pressure reduction.

In addition, when RF bias is increased from 100 V to 325 V, the height of micro-masking reduces from 56 μm to 16 μm. The reason of micro-masking reduction is the enhancement of ion bombardment. Figs. 3 and 4 show the bottom images of TSV before and after RF bias enhancement, respectively.

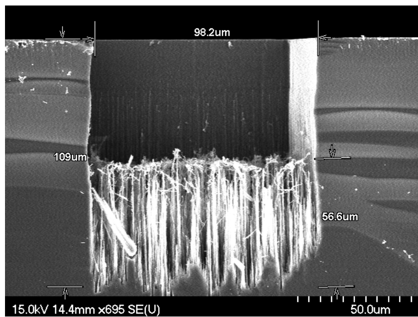

Fig. 3 The bottom of TSV before RF bias power enhancement.

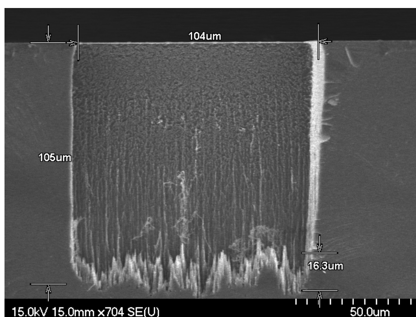

Fig. 4 The bottom of TSV after RF bias power enhancement.

3.2 Micro-masking removal by adjusting parameters during etching

In this study, three different recipes are developed for TSV etching. Each recipe shows no micro-masking issue inside TSV. TSV morphology using recipe A shows isotropic etching seriously since sidewall protection layer was bombarded by argon ion at high bias power. In recipe B, a tapered profile was formed due to high SF_6 concentration. This profile can increase step coverage and form conformal copper seed layer for the successful electroplating. Recipe C shows the vertical shape of high aspect ratio by carefully setting SF_6 and bias power. Figs. 5(a)-(c) show 50-μm TSV profiles using three recipes.

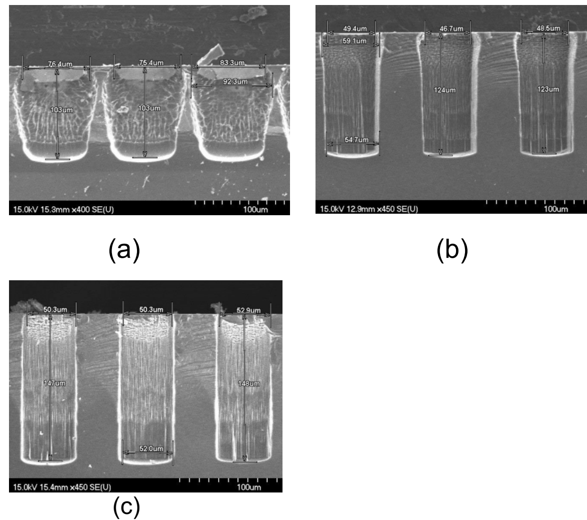

Fig. 5 TSV profiles of (a) recipe A, (b) recipe B, and (c) recipe C.

4 Conclusion

Bosch process can be applied for etching high aspect ratio silicon vias. However, micro-masking issue happens if the etching recipe is not properly controlled. This study shows isotropic etching after Bosch process or parameter adjustment during Bosch process can achieve a micro-masking free profile.

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