Substrate Noise Suppression Technique for Power Integrity of TSV 3D Integration

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***Abstract*—In this paper, a substrate noise suppression technique is proposed for the power integrity of TSV 3D integrations. This substrate noise suppression technique reduces both substrate and TSV coupling noises using active substrate decouplers (ASDs) to absorb the substrate noise current. Additionally, the ASD placing is also presented to suppress noises effectively for different 3D structures. For a processor-memory stacking integration, the ground bouncing noises can be reduced by 44.1% via the noise suppression technique. The proposed substrate noise suppression technique can enhance the power integrity of TSV 3D-ICs by reducing the coupling substrate noises.**

I. Introduction

Three-dimensional (3D) integration technology can provide enormous advantages in achieving multi-functional integration, microminiaturizing form factor, improving system speed and reducing power consumption for future generations of ICs. In addition, through-silicon-via (TSV) has emerged as a solution in developing 3D integration [1]. However, stacking multiple dies would face a severe challenge of the power integrity due to the increasing current density and parasitic impedance in TSV 3D-ICs [2]. Therefore, we used active DECAPs to suppress simultaneous switching noises from packages [3]. The active DECAPs significantly affect the design of the power/ground (P/G) networks in TSV 3D integration.

In addition to the simultaneous noise from package, large coupling noises, such as ground bounce noises and substrate noises, are also coupled from the shared substrate or TSVs [1]. In view of this, noise suppression will become a critical design issue in TSV 3D heterogeneous integrations. In this paper, a substrate noise suppression technique using active substrate decouplers (ASDs) is presented for power integrity of TSV 3D-ICs. The proposed substrate noise suppression technique can significantly reduce the noises coupled from TSVs and silicon substrates under different 3D structures.

II. Substrate Noise Analysis and Modeling in TSV 3D Integration

In TSV stacked 3D-ICs, large coupling noises are induced by the increasing current density. The fast state transitions in digital circuits induce substantial switching noises that are coupled to analog circuits through the silicon substrates. Fig. 1 shows two propagation paths of the coupling noises, which

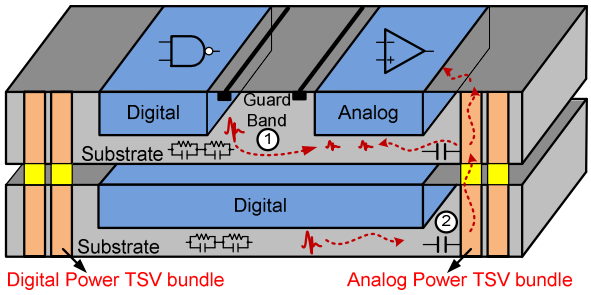

Fig.1. Two propagation paths of substrate noises in 3D ICs.

degrade the power integrity in heterogeneous integration significantly. On Path-1, the shared silicon substrate provides a noise transmission medium because of the substrate contact and parasitic junction capacitances. Moreover, this conductive path is the major noise propagation path for mixed-signal circuits in system-on-chip (SoC) and TSV 3D-ICs. In addition to the conductive substrate, another noise propagation path in TSV 3D-ICs is from the substrate of digital circuit to the analog power TSVs as Path-2. The S_iO_2 layer surrounding TSV for DC isolation results in the high parasitic capacitance between the TSV and the silicon substrate. Hence, the noises from the silicon substrate can be coupled to the TSV through the large capacitance [1].

The power TSV bundle can be modeled through via extraction parameters of resistance, inductance, and capacitance [4]. The TSV characteristics of height, size, and pitch are 50μm, 25μm, and 50μm, respectively. In addition to the power TSV bundle, the silicon substrate is modeled as a mesh topology, where the resistance is 15Ω and capacitance is 5fF [5]. By considering the realistic coupling effect between TSVs and silicon substrates, the substrate model is modified using the parasitic capacitance to couple noises between TSVs and silicon substrates.

III. Active Substrate Decoupler (ASD) Design

To suppress the substrate noises and bouncing noises, an ASD is designed using a noise suppression amplifier [6] as shown in Fig. 2. The ASD consists of an operational amplifier and a negative feedback capacitor. The negative input and positive input of the operational amplifier are connected to the substrate and the quiescent ground, respectively. This amplifier virtually shorts the substrate to the reference ground and keeps the shared substrate quiescent. Additionally, the

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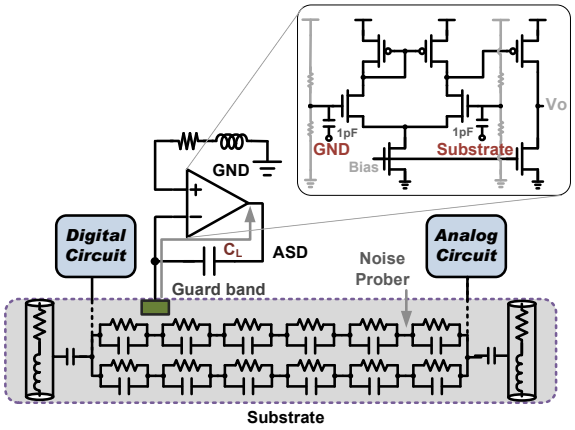

Fig.2. Schematic of active substrate decoupler (ASD).

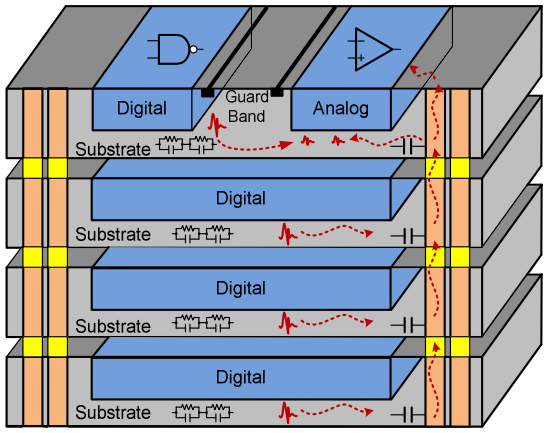

Fig.3. Block diagram of mixed-signal circuit in TSV 3-D integration.

output and negative input of the operational amplifier are connected as a negative feedback loop using a decoupling capacitor, C_L, which is set as 10pF. This capacitance is multiplied by the voltage gain through Miller multiplication effect. Hence, more substrate noise current can be further absorbed by the decoupling capacitor.

The differential inputs of ASD are DC biased at 660mV, and AC coupled with the substrate or reference ground by a small capacitor (1pF). Based on UMC 65nm CMOS SP technology, the simulation results show that the DC gain, −3dB frequency, and power dissipation are 28dB, 404MHz, and 313μW, respectively. Moreover, multiple ASDs connected in parallel can further achieve great noise reduction. However, a trade-off exists between the area overhead and noise suppression efficiency.

IV. ASD Placing for Noise Suppression

In TSV 3D-ICs, the performance of sensitivity analog circuits would be degraded since large simultaneous switching noises are induced by the fast switching in digital circuits and coupled to analog power TSVs. For the power integrity of TSV 3D-ICs, the substrate noise suppression technique with ASD placing is described in this section. Consequently, inverter matrix and differential amplifiers are utilized as digital circuits and analog circuits based on UMC 65nm CMOS technology.

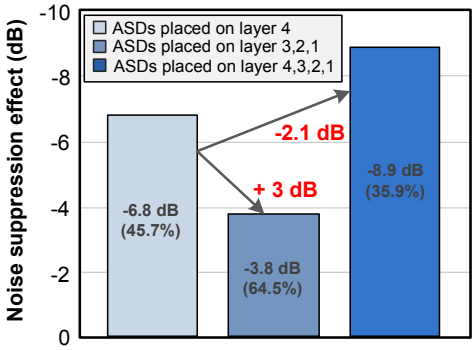

Fig.4. Noise suppression effect of ASD planning for mixed-signal circuit in 3D structure.

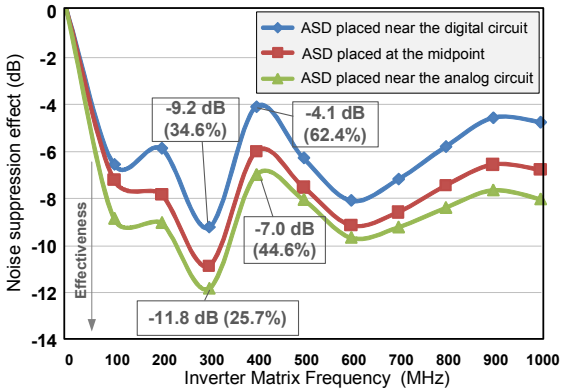

Fig.5. Noise suppression effect on mixed-signal layer.

A. Mixed-Signal Layer in TSV 3D Integrations

A TSV 3D integration with a mixed-signal layer is illustrated as shown in Fig. 3. The structure of this 3D integration is extended to four stacked layers, consisting of 1 mixed-signal layer and 3 digital layers. The mixed-signal circuit is placed on the top layer as Layer 4. For the analog circuitry, the power noises are propagated from the substrate and analog power TSVs.

For the ASD placing, three ASDs are placed on Layer 4 because the conductive path from the substrate is the major noise propagation path. For Layer 1-3, one ASD is placed on each digital layer. According to the ASD placement of each layer, different scenarios of the ASD placing are compared as shown in Fig. 4. The noise suppression effect is defined as the ratio between the RMS voltage of the power noise with ASDs and that without ASDs. Placing 3 ASDs on the mixed-signal layer can achieve more noise reduction (+ 3dB) compared to 3 ASDs placed on three digital layers. Moreover, extra 2.1dB noise reduction can be achieved using 6 ASDs (3 ASDs on Layer 4 and 3 ASDs on Layer 1-3). In view of these, placing ASDs on mixed-signal layer can reduce power noises significantly.

For the ASD placing on the mixed-signal layer, three ASDs are placed at various locations on the mixed-signal layer, including near the noise source, at the midpoint of digital and analog circuit, and near the sensitive analog circuit. The noise suppression effects of the ASD placing on the mixed-signal layer are as shown in Fig. 5. The maximum suppression effects are -11.8dB and -9.2dB with placing ASD

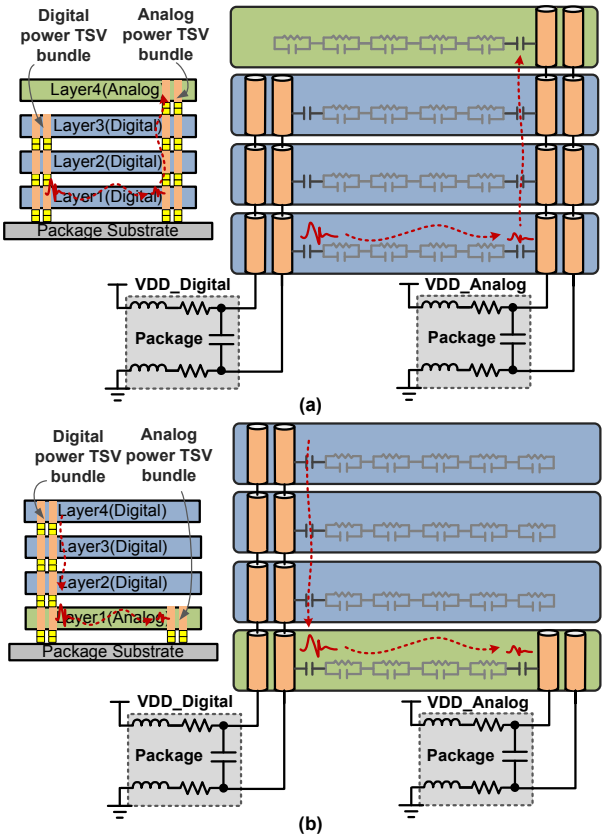

Fig.6. TSV in 3-D integration. (a) Analog circuit on the top layer. (b) Analog circuit on the bottom layer.

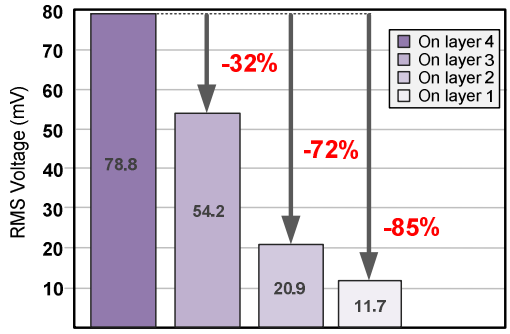

Fig.7. Noise comparison with different analog layer.

near the analog and digital circuit at 300MHz, respectively. Placing ASDs near the analog circuit can realize the largest noise suppression effect compared to other ASD placements. Moreover, the noise suppression effect for placing ASDs near the analog circuit is almost 2dB larger than that near the digital circuit over 100MHz to 1GHz. Therefore, placing ASDs near the analog circuit is effective to reduce the power noise of the sensitive analog circuit. The substrate noise can be eliminated significantly while the ASDs are placed close to the sensitive circuits, not close to the noise source. This phenomenon results from the characteristic of virtual shorting of ASD. Additionally, the ASD placing on the mixed-signal layer is not only suitable for TSV 3D-ICs but SoC applications.

B. Separated Analog Layer in TSV 3D Integrations

TSV 3D structures with separated digital and analog layers are illustrated as shown in Fig. 6, a four-layer stacking

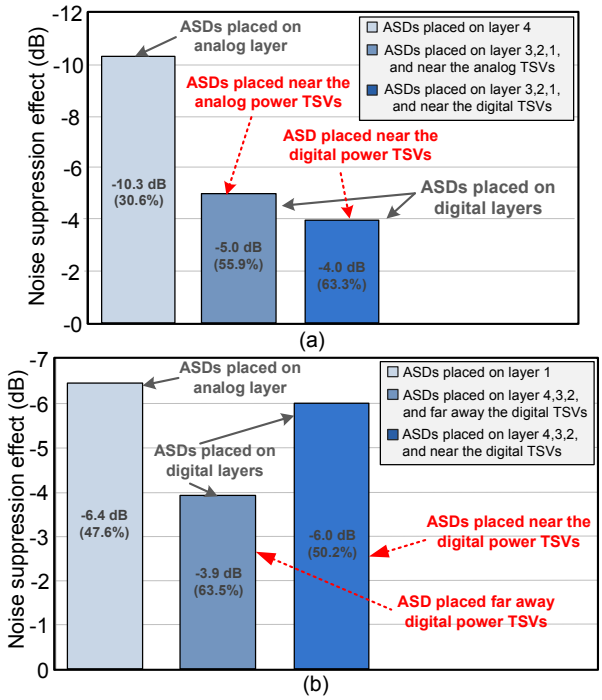

Fig. 8. Noise suppression effect (a) Analog circuit on the top layer. (b) Analog circuit on the bottom layer.

structure with one analog layer and three digital layers. The noise propagated from the shared substrate does not exist in these structures. However, the simultaneous noises are propagated through the analog power TSV to the analog circuits. The noise propagation paths are related to the stacking order of the analog layer in TSV 3D-ICs. Fig. 7 shows the noise comparisons with different orders of the analog layer. Clearly, the analog layer placed as the bottommost stratum can achieve a most significant substrate noise reduction because of the long noise propagation path and the small impendence of analog power TSVs.

Figs. 6(a) and 6(b) present the block diagrams of placing analog layer at the top (worst case) and at the bottom (best case), respectively. For the ASD placing, three ASDs placed on the analog layer and distributed to other digital layers are realized. Fig. 8 shows the comparisons of noise suppression in both best and worst cases. Three ASD are distributed to each digital stratum and placed near either the digital TSV bundles or analog TSV bundles. The noise suppression effect for the worst case can achieve -10.3dB while the three ASDs are placed within the analog layer. On the other hand, the noises are suppressed to -5.0 dB when the ASDs are distributed on the other three digital layers near the analog power TSVs. Additionally, the noise suppression effect increases from -4.0dB to -5.0dB when the ASDs move from the vicinal region of digital power TSVs to analog power TSVs. The simulation results for the best case are similar than those for the worst case as shown in Fig. 8(b). Nevertheless, moving the ASDs from the vicinal region of digital power TSVs to analog power TSVs decreases the noise suppression effect from -6.0dB to -3.9dB. In view of this, ASDs should be distributed on the noise propagation path near the sensitive circuits.

Table 1: ASD placing under different TSV 3D structure.

Mixed-Signal 2D ICs	Place ASDs near analog circuits	
TSV 3D-ICs (Mixed-Signal Layer)	Rule 1: Place ASDs in MS layers Rule 2: Place ASDs near analog circuits	
TSV 3D-ICs (w/o mixed-signal layer) (TSV coupling noises)	Suggestion: Analog layer at the bottom layer	
	Analog layer at top layer	Place ASDs near analog power TSVs in each layer
	Analog layer at bottom layer	Place ASDs near digital power TSVs in each layer

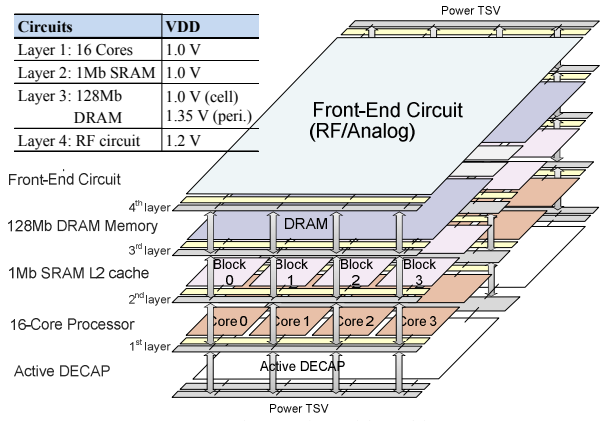

Fig. 9. Heterogeneous TSV 3D integration with multi-core, SRAM, DRAM, front-end circuits stacking.

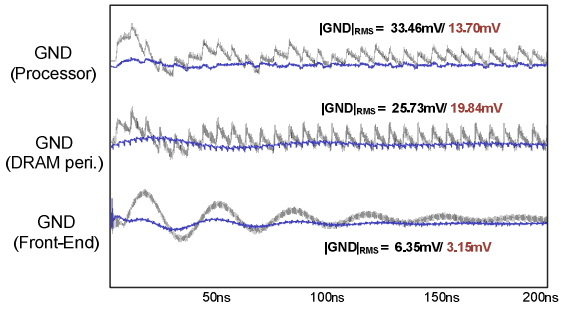

Fig. 10. Waveforms of ground noises with(blue)/without(gray) ASDs.

C. *ASD Placing in TSV 3D Integrations*

With different 3D structures, the distribution of ASDs affects the efficiency of the ASD placing. The guideline of ASD placing is that ASDs should be distributed on the noise propagation path near the sensitive circuits. Table 1 lists some helpful information of the ASD placing according to different 3D structures. Since the noise propagated within a layer is larger than other noises coupled from other layers, ASD should be placed on the mixed-signal layer near analog circuits to achieve significant noise reduction. Consequently, for effectively reducing the coupled noises between layers, placing ASDs near the analog/digital power TSVs can achieve noise suppression effect significantly while the analog layers are stacked on the top/bottom layers, respectively.

V. Case Study for TSV 3D Integration

To demonstrate the substrate noise suppression technique for the power integrity in the TSV 3D integrations, a heterogeneous TSV 3D integration of processor-memory stacking is developed as shown in Fig. 9. The heterogeneous integration consists of a 16-core processor tier with distributed L1 caches, a SRAM tier (1MB L2 cache), a DRAM tier (128Mb), and an analog front-end RF tier. This TSV 3D integration with the hierarchical memory system alleviates the memory wall problem and increases the throughput of the multi-core system. Depending on the power information in [7-10], the feasible supply voltages of each layer in this TSV 3D integration are also list in Fig. 9. The maximum power consumption of the multi-core processor, SRAM based L2 cache, DRAM memory, and RF circuits are 1.6W, 0.36W, 1.5W, and 0.25W, respectively. And the ratio between the dynamic power and static power is set around 7:3.

8 ASDs are distributed around the ground TSVs in each layer to reduce the coupling noises. Fig. 10 presents the simulation waveforms of three ground supplies. By absorbing the substrate noise current and virtually shorting to reference ground, ASDs keep the ground supplies quiescent. The noise reductions of ground supplies for processor, DRAM peripheral circuits, and RF circuits are 59.05%, 22.89%, and 50.40%, respectively. The power overhead of the ASDs is 13.17 mW which is only occupied 0.35% of the total power consumption.

VI. Conclusions

In this paper, a substrate noise suppression technique is presented for TSV 3D-ICs by considering both substrate and TSV coupling noises. This substrate noise suppression technique reduces noises using ASDs that utilizes a decoupling capacitor to absorb the substrate noise current. For further achieving effective noise reduction, the ASD placing is also presented for different 3D structures. Therefore, the proposed technique can enhance the power integrity of TSV 3D-ICs.

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