

# Subthreshold Asynchronous FIFO Memory for Wireless Body Area Networks (WBANs)

Yi-Te Chiu, Ming-Hung Chang, Hao-Yi Yang, and Wei Hwang  
 Department of Electronics Engineering & Institute of Electronics, and  
 Microelectronics and Information System Research Center (MIRC)  
 National Chiao-Tung University, Hsinchu 300, Taiwan

**Abstract**—In this paper, a 512-word by 16-bit (8kb) subthreshold asynchronous first-in first-out (FIFO) memory is proposed for wireless body area networks (WBANs). For the ultra-low power consideration, a novel ultra-low power subthreshold 8-transistor (8T) SRAM cell is presented, which improves write margin and reduces write variation in subthreshold regime. Reverse short-channel effect (RSCE) is utilized in read-buffer and write access transistor to improve read/write ability. In addition, an adaptive write-word-line control scheme is proposed for lower write power and process-voltage-temperature (PVT) tracking. The proposed FIFO is implemented to achieve a minimum operating voltage of 400mV in UMC 65nm technology, with merely 1.05 $\mu$ W power consumption at 5MHz reading frequency and 200kHz writing frequency.

## I. INTRODUCTION

FIFO (First in, First out) memories are widely used as data flow buffers in the communication system. An example is the emerging WBAN, a breakthrough personal healthcare technology for body condition monitoring and diagnosis. A conventional FIFO memory consists three major parts, storage elements, read/write pointers, and the read/write control circuitry. The storage element may be register, latch, or SRAM cell. For the consideration of high density and low power, dual-port SRAM based FIFO is applicable. As the low sample rate of medical sensor and high transmission rate, the asynchronous FIFO memory slows down the write frequency for lower write dynamic power and speeds up the read.

To achieve high reliability and longer battery life for portable electronic products and medical instruments, high Static Noise Margin (SNM) and low power FIFO memory is required. Due to loose timing constraint of the wireless sensor node, subthreshold supply voltage is suggested to be an effective method to gain ultra-low power operation. However, exponential effect of threshold voltage variation, the reduction of signal level, and the degradation of  $I_{on}$ - $I_{off}$ -ratio are the critical issues of subthreshold circuitry. Threshold voltage shift due to random dopant fluctuations and processing variation causes the sideways offsets [1]. In addition, the reduction of signal level directly hurts the noise margin of logics. The degradation of the  $I_{on}$ - $I_{off}$ -ratio limits the sharing elements of the array logic such as the memory element. All of the subthreshold voltage effects are considered in this work.

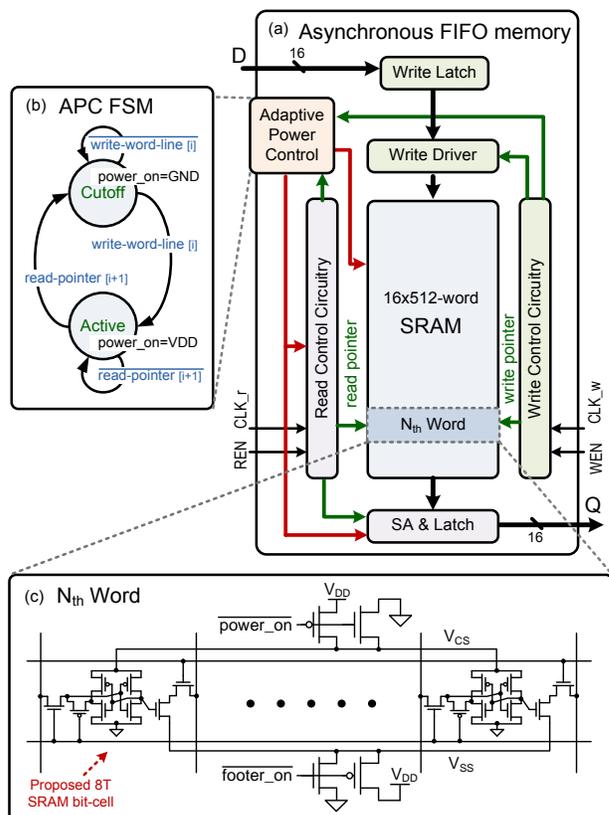


Figure 1. (a) Block diagram of proposed FIFO memory. (b) FSM of self-adaptive power control. (c)  $N_{th}$  word of storage element.

In section II, ultra-low power design technique of proposed asynchronous FIFO is described. The self adaptive power control system proposed in our previous work [8] is illustrated. In section III, conventional dual-port SRAM limitation is discussed. Section IV describes proposed 8-transistor (8T) SRAM operation and read/write ability improvement. In section V, simulation comparison is made among existing SRAMs. Section VI makes the conclusion.

## II. ULTRA-LOW POWER ASYNCHRONOUS FIFO WITH SELF-ADAPTIVE POWER CONTROL

As shown in Fig. 1(a), the asynchronous FIFO composes of

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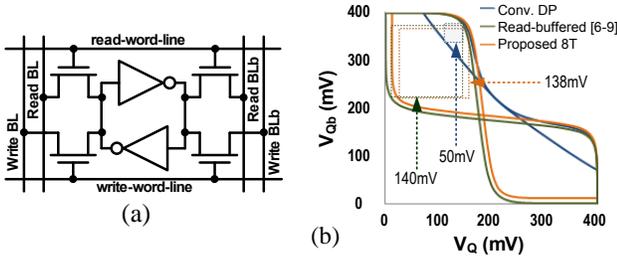


Figure 2. (a) Conv. dual-port SRAM (b) Read SNM butterfly curve

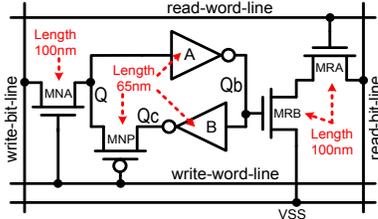


Figure 3. Proposed 8T SRAM

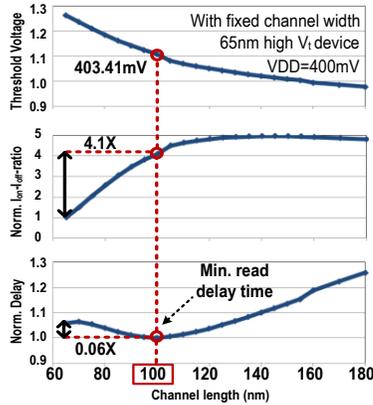


Figure 4.  $V_t$ ,  $I_{on}$ - $I_{off}$  ratio, and delay versus channel length

read/write pointers, read/write control circuitries, self-adaptive power control system, and SRAM-based storage elements. Read/write pointers are used as address pointers of FIFO memory. An effective way to construct a logic pointer is the utilization of shift registers. The use of shift registers eliminates the use of counters and decoders, which reduces power consumption and increase operation speed significantly. Asynchronous clock signals,  $CLK_r$  and  $CLK_w$ , are connect to the read/write control circuitries with clock gating.

Since the status of all the words in FIFO memory is predicable due to first-in first-out data behavior, a self-adaptive power control system, which cutoff the power supply of don't care words, could be utilized to efficiently reduce power consumption. The power gating circuit is inserted in each word of the FIFO memory. Fig. 1(b) shows the finite-state machine of the power gating signal,  $power_{on}$ . In the beginning, each word is in *cutoff state*, where it consumes just 1.7nW. Whenever the accessed word is going to write, it changes to active state and the cell supply of the word is charged to VDD. Each written word stays in *active state* until the word-data is read out.

### III. DUAL-PORT SRAM CELL LIMITATION

The most common method to measure the stability of SRAM cells is hold/read static noise margin (HSNM/ RSNM),

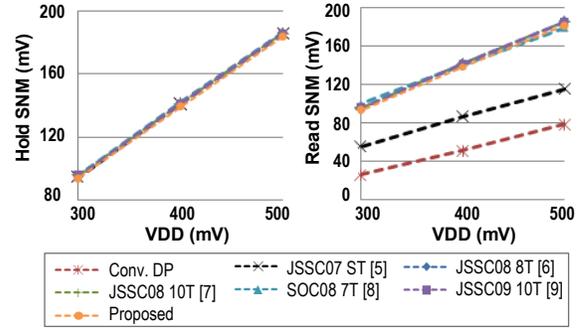


Figure 5. Read/hold SNM comparison

which is the DC voltage noise tolerated in hold/read operation without flipping the storage node. The conventional dual-port SRAM (Fig. 2(a)) fails to operate in subthreshold because of read disturb induced read SNM lowering under reduced signal level and increased variation.

As technology and supply voltage scaling down, the write margin of conventional SRAM becomes limited. The write-ability could be improved by using lower cell supply voltage [6], boosting the write-word-line voltage [9], or applying negative voltage on write-bit-line [4]. Nevertheless, these methods cost overhead power and area due to adding control circuits or boosting capacitance.

### IV. PROPOSED SUBTHRESHOLD 8T SRAM

In this work, a novel 8T SRAM cell (Fig. 3), which consumes ultra-low power in read/write operation as well as stand-by period in subthreshold regime, is proposed. All of the MOSFETs are high- $V_t$  devices so that the leakage currents are diminished. Read-buffer,  $MRA-MRB$ , and write access transistor,  $MNA$ , utilize RSCE to reduce  $V_t$  for better performance. The pass transistor,  $MNP$ , is utilized to cut off the feedback loop of the inverter pair during write operation. In super- $V_t$  regime,  $V_t$  drop of  $MNP$  causes critical leakage currents not to mention short-circuit currents if the inverter pairs are not sizing appropriately [2]. However, in subthreshold regime, the voltage drop of  $MNP$  is tiny and so is the leakage current.

#### A. Read-SNM and Read-Ability Improvement

Since the read-buffer ( $MRA-MRB$ ) keeps the storage node away from disturb noise and eliminates the read SNM limitation, read SNM butterfly curve of proposed 8T SRAM is nearly equal to the hold SNM curve of that. Fig. 5 shows read/hold SNM of different SRAMs [5-9] versus supply voltage. Although proposed 8T SRAM has a pass transistor ( $MNP$ ) between the inverter pair, read/hold SNM of proposed 8T SRAM is tiny drop comparing to those of read-buffered SRAMs [6-9] (Fig. 2(b)).

That the read-buffer of proposed 8T SRAM utilizes RSCE improves  $I_{on}$ - $I_{off}$ -ratio. Higher  $I_{READ}$ - $I_{LEAKAGE}$ -ratio enhances not only the capacity of each read-bit-line but also the margin of sense amplifier. Since  $V_t$  random variation,  $\sigma V_t$ , is inverse proportional to the square root of the product of channel length and width [3]. Therefore, larger channel length decreases the impact of local  $V_t$ . In subthreshold regime, increasing device lengths can have a significant impact on

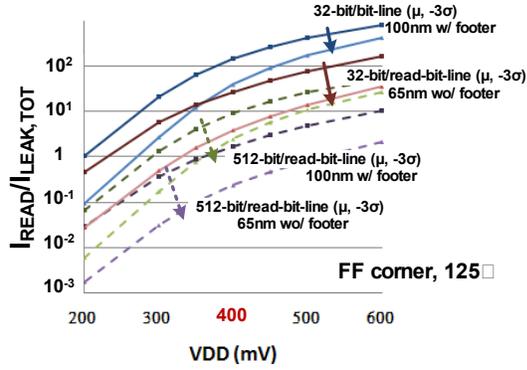


Figure 6.  $I_{READ}/I_{LEAKAGE,TOTAL}$ -ratio (mean and  $-3\sigma$  contour) of 512-bit and 32-bit per read-bit-line with/without RCSE and footer respectively.

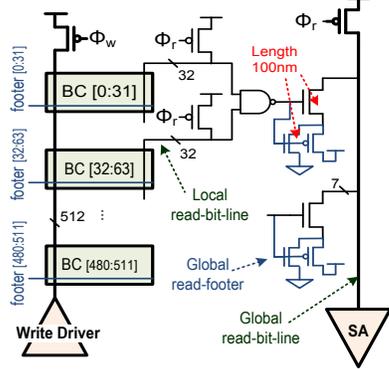


Figure 7. Read scheme with hierarchical read-bit-lines tolerates PVT variation in sub- $V_t$  regime

increasing even the mean read current since the RSCE essentially causes a decrease in the effective  $V_t$  [1]. As can be seen in Fig. 4, increasing the channel length decreases  $V_t$  and increases  $I_{on}/I_{off}$ -ratio. The channel length of 100nm makes the minimum read delay time and 4.1X improvement of  $I_{on}/I_{off}$ -ratio.

To further improve the ratio of  $I_{READ}/I_{LEAKAGE}$ , read-buffer-footers are attached to the foot of each read-buffer in all words. During read operation, all foots of read-buffers remain at  $V_{DD}$  except the accessed word, foots of which are pulled to GND. Therefore, the leakage currents of the read-buffers are diminished. It can be seen from Fig. 6 that the  $I_{READ}/I_{TOTAL\_LEAKAGE}$ -ratio is improved by using read-buffer-footers and longer channel length (100nm) of read-buffer. In the read circuitry, the hierarchical read-bit-lines scheme (Fig. 7) enlarges sensing margin and tolerates PVT variation in subthreshold regime. Each local read-bit-line contents 32-bit-cells. The global read-bit-line will be discharged by footed read-buffer, utilizing RSCE, whenever one of local read-bit-lines is discharged.

### B. Write -Ability Improvement

The proposed 8T SRAM cell greatly enhances the write-ability in subthreshold regime. The proposed 8T SRAM cell enlarges the write margin by cutting off the positive feedback loop of inverter pairs with no peripheral circuit. As soon as coming to write operation, write-word-line turns on  $MNA$  and turns off  $MNP$  simultaneously. The data wants to write would be pass through  $MNA$ , inverter  $A$  and  $B$  to the node  $Qc$ .  $MNA$

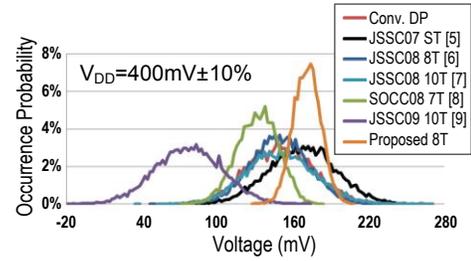


Figure 8. Distribution of write margin in Monte Carlo Simulation

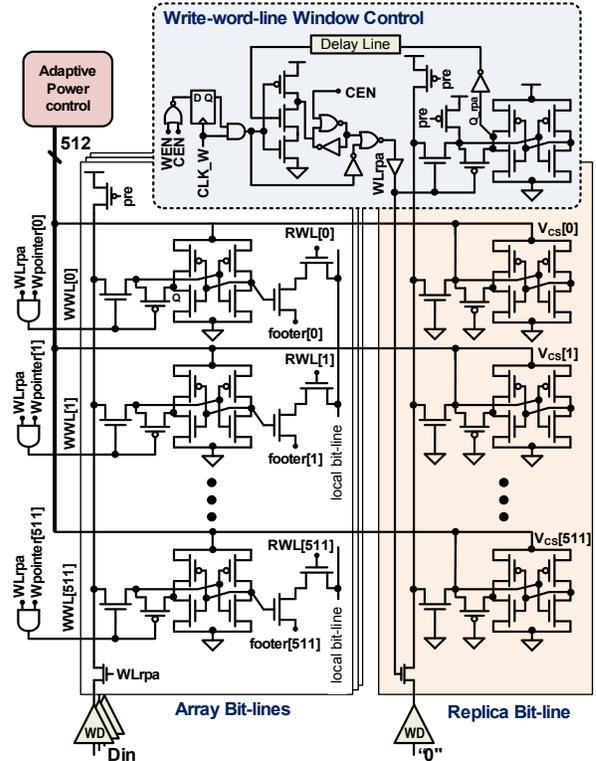


Figure 9. Replica bit-line controls write-word-line window for low write power and PVT tracking.

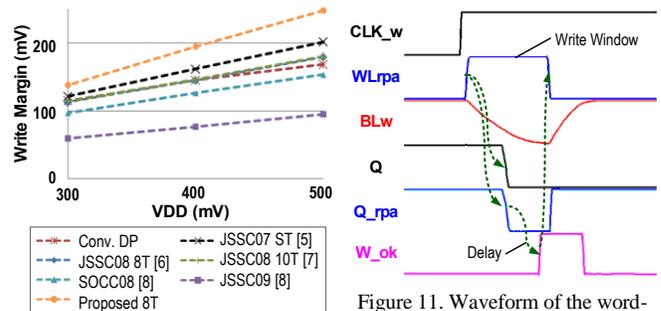


Figure 10. Write margin comparison

Figure 11. Waveform of the word-line window control

utilize RSCE to lessen  $V_t$  for better write margin. Fig. 8 shows Monte Carlo simulation (10000 times) of write margin of proposed 8T SRAM and the other SRAMs. It shows that the proposed 8T SRAM cell has better write-ability and less variation than the others.

### C. Write Power Minimization

The scheme of single-end write port of the proposed 8T SRAM cell reduces the active power during write operation.

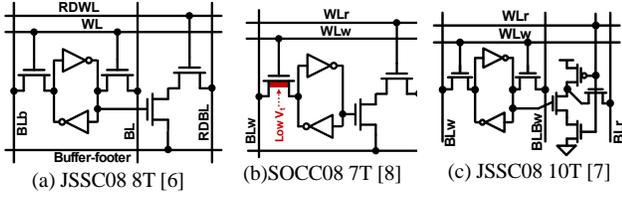


Figure 12. Dual-port SRAM cells

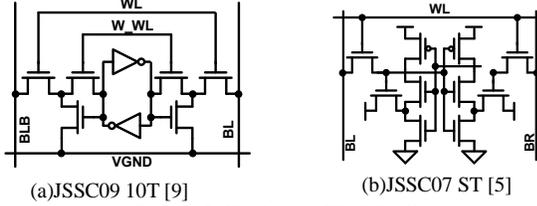


Figure 13. Single-port SRAM cells

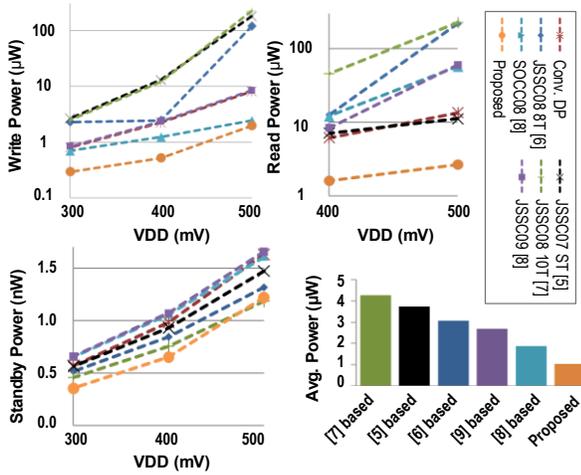


Figure 14. Read power (@ 5 MHz, 25°C), write power (@ 200 kHz, 25°C), standby power (25°C), and average power comparison

TABLE I. Summary of the FIFO memory features.

Technology	UMC 65nm CMOS
Supply voltage	400mV
Memory size	512-word by 16-bit (8kb)
Read / Write frequency	5MHz / 200kHz
Power consumption	1.05µW
Standby leakage current	1.64µA

For a conventional SRAM memory, power dissipated in bit-lines represents about half of the total active power consumption during a write operation since the word-line, connecting a large amount of bit-cells, is one of the largest capacitive parts of the memory.

A write-word-line window control scheme is proposed to open an adaptive write window to minimize write active power (Fig. 9). The waveform of the signals in a write operation is shown in Fig. 11. In a write operation,  $WL_{rpa}$  turns on initially. It turns on both the write-access-transistor of duplicate cell in the window control block and the accessed write-word-line,  $WWL[i]$ . The data,  $Din$ , then writes to accessed word. In the same time, the replica bit-line, where all the cells are hardwired to “1”, writes “0” to the duplicate cell, since it’s the worst circumstances of write delay. After the

duplicate cell is written “0” successfully,  $W_{ok}$ , delayed by a delay line for wider window margin, disables the write-window. The self-adaptive power control system cutoffs the power supplies of cells in replica bit-line in don’t care words. The replica bit-line adaptively controls write-word-line window so that the write operation consumes ultra-low power in high reliability.

## V. SIMULATION RESULTS

Tolerating -25°C to 125°C temperature variation and all process corners, the 8kb asynchronous FIFO is implemented in UMC 65nm technology with 400mV supply voltage and 5MHz/200kHz read/write frequency, shown in TABLE I. Read/Write/Standby/Average power of the proposed design, compared between existing dual-port (Fig. 12) and single-port (Fig. 13, unable to simultaneously read/write operation) SRAM [5-9] based FIFO memories are shown in Fig. 14. With 400mV supply voltage, the proposed design consumes the minimum read/write/standby power (1.61µW/0.52µW/8.68nW) among the other SRAM designs (Fig. 14). With the same average power estimation in previous work [8], (The simultaneous read/write power is neglected in single-port) the proposed design has only 1.05µW average power consumption, which reduces 44.1% over the previous work.

## VI. CONCLUSION

A robust subthreshold asynchronous FIFO memory with self-adaptive power control is proposed in this paper. A novel 8T SRAM cell is proposed to improve write margin and to reduce write variation. RSCE is utilized to decrease  $V_t$  and to rise  $I_{on}$ - $I_{off}$ -ratio. For improving read/write ability, hierarchical read-bit-lines and write window control replica bit-line are proposed. All above presented FIFO memory design techniques enable ultra-low power and robust operation for WBAN applications.

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