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Thermal Control Mechanism with In-Situ Temperature Sensor for TSV 3D-ICs

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***Abstract*- In TSV (through-silicon-via) 3D-ICs, stacking multiple dies faces a severe challenge of the thermal effect due to the low thermal conductivity of inter-layer dielectrics and high power density. In this paper, a thermal control mechanism with an in-situ temperature sensor for TSV 3D-ICs is proposed using thermal guard rings and thermal TSVs. Depending on the thermal guard ring and thermal TSVs, an analytical model for on-chip heat dissipation in each power-thermal domain is also presented in this paper. Based on the analytical model, the offset temperatures between the hotspots in the power-thermal domain and thermal guard ring can be calculated. Therefore, the in-situ temperature sensor is placed near the thermal guard ring to detect the temperature and feedback the thermal information for the system. The simulation results show the thermal control mechanism with an in-situ temperature sensor can reduce temperature and detect heat dissipation of TSV 3D-ICs significantly. This technique can be extended to balance workloads in the overall system for further reducing temperature.**

I. INTRODUCTION

Moore's law describes a long-term trend in the history of integrated circuit technology, in which the number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years. However, Moore's Law will ultimately hit a brick wall as the lithography techniques become limited by the wavelength of light. Hence, three-dimensional (3D) integration is regarded as the solution to keep the pace with the performance improvement projected by Moore‘s law. 3D integration technology can provide enormous advantages in achieving multi-functional integration, microminiaturizing form factor, improving system speed and reducing power consumption for future generations of ICs [1]. Among different 3D technologies, through-silicon-via (TSV) has emerged as a solution in developing 3D integration [2]. However, stacking multiple dies would face a severe challenge of the thermal effect due to the low thermal conductivity of inter-layer dielectrics and high power density [3]. Although the power consumption of a die within a 3D-IC is expected to be decreased due to the shorter interconnects, the heat removing of a 3D-IC is much more difficult than that of a 2D-IC. The cause is that the ambient environment of the die of a 2D-IC is the cooling material, but the ambient environment of a die within a 3D-IC may be another die which also generates heat. In 3D-ICs, because of the poor thermal conductivity of the inter-layer dielectrics layers, the heat generated by the devices cannot be effectively dissipated toward the heat sinks. Therefore, the thermal issue of a 3D-IC is much severer than that of a 2D-IC.

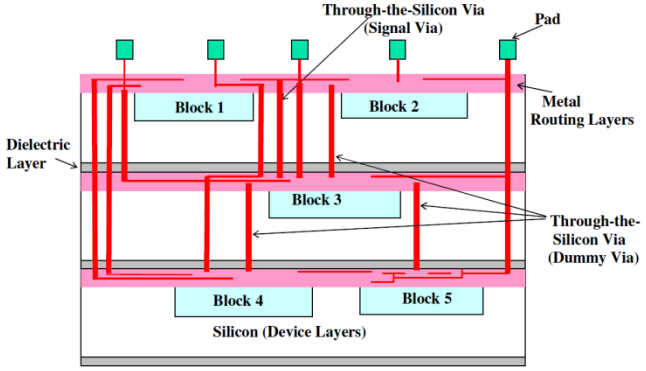

Fig. 1. Cross-Section of a TSV 3D-IC with thermal TSVs. [4]

There are two kinds of circuit cooling schemes for 3D-ICs, including heat sink optimization methods and internal heat distribution optimization methods [4]. Heat sink optimization methods, such as air cooling by electrical fans, micro-channel cooling at heat sinks, etc., are often targeted at cooling down the heat sink of a chip. In addition, since vertical TSVs are effective thermal conductors to eliminate localized hot spots, several temperature-aware physical design schemes were investigated to reduce temperature using thermal TSVs as shown in Fig. 1 [4-7]. These schemes often assume a perfect heat sink which can always be cooled down to certain low temperatures, and change the internal structure of the circuit for better heat dissipation, such as the locations of the devices, thermal TSV insertion, micro-channel insertion [8, 9]. However, electrical fans and micro- channel cooling scheme is usually very costly to fabricate, and the micro-channels will also create large obstacles for the TSVs.

The internal heat distribution optimization methods are presented to re-distribute the heat sources. Since macro

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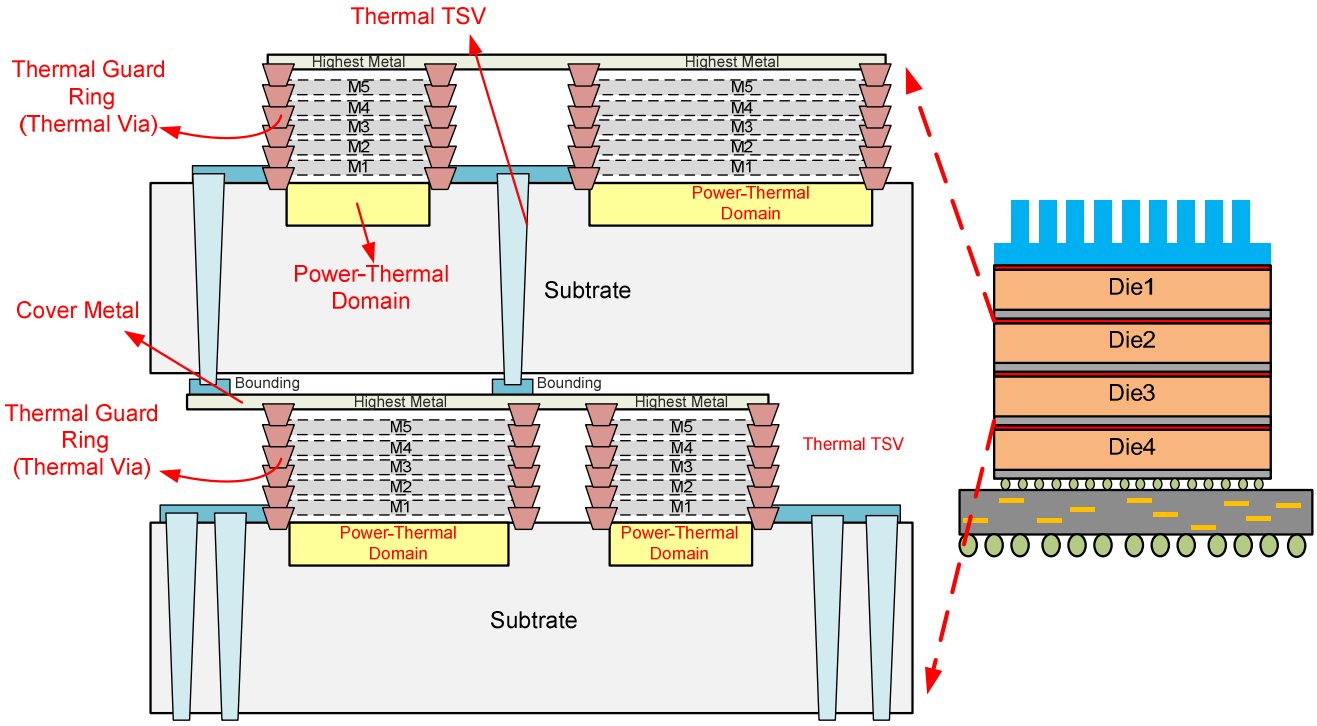

Fig. 2. Thermal control mechanism for TSV 3D-ICs is proposed using thermal guard rings, a cover metal and thermal TSVs.

blocks and cells are the major heat sources in a circuit, the positions of the blocks and cells will affect the circuit temperature. One approach of TSV 3D-IC thermal optimization effort was applying thermal-driven 3-D floor-planning and placement [10-12]. However, even after thermal-driven floor-planning or thermal-driven placement, the maximum temperature can still be as high as 150°C, which is too high for a circuit to operate properly.

In this paper, a thermal control mechanism with an in-situ temperature sensor for TSV 3D-ICs is proposed using thermal guard rings and thermal TSVs. The circuits of each layer would be divided into several power-thermal domains which are surrounded by power rings and thermal guard rings. Moreover, depending on the thermal guard ring and thermal TSVs, an analytical model for on-chip heat dissipation in each power-thermal domain is also presented in this paper. Based on the analytical model, the offset temperatures between the hotspots in the power-thermal domain and thermal guard ring can be calculated easily. The remainder of this paper is organized as follows. Section II presents the thermal control mechanism with thermal guard rings and thermal TSVs. The analytical model for on-chip heat dissipation in each power-thermal domain is presented in Section III. The configuration of TSV 3D-ICs for the thermal analysis is described in Section IV. Section V shows simulation results. Finally, Conclusions are given in Section VI.

II. Thermal Control Mechanism for TSV 3D-ICs

Thermal TSVs are very effectively for heat dissipation. However, thermal TSVs are costly to fabricate, and the yield would be degraded with the increasing number of TSVs. In addition, the pitch of TSVs is much larger than that of metal

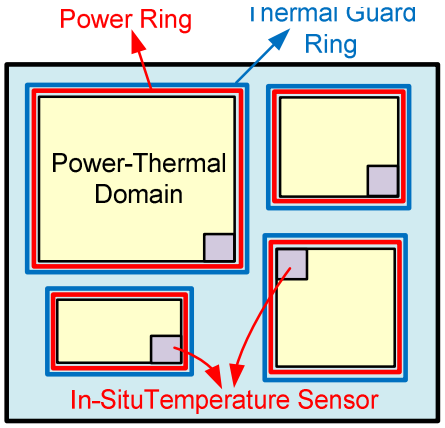

Fig. 3. Power-thermal domains with in-situ temperature sensors.

wires. In 3D-IC structures, the thermal TSVs are placed at the whitespace between two macro blocks on each layer. Therefore, the thermal TSVs may not be placed near the heat sources, and the efficiency of the heat removing would be decreased. In view of these, a thermal control mechanism for TSV 3D-ICs is proposed using thermal guard rings, a cover metal and thermal TSVs. Fig. 2 presents the concept of the thermal control mechanism. The thermal guard rings and the cover metal are constructed to provide heat dissipation paths from heat sources to the thermal TSVs. Moreover, the heat can be further removed through the thermal TSVs to the cooling package.

The circuits on each layer in 3D-ICs would be divided into several power-thermal domains which are surrounded by the power rings and thermal guard rings as shown in Fig. 3. Each power-thermal domain contains an in-situ temperature sensor near the thermal guard ring to detect the temperature

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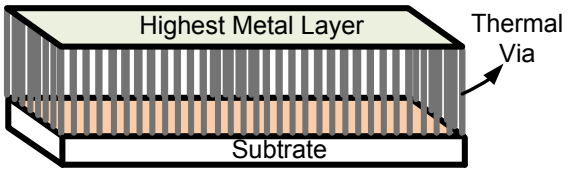

Fig. 4. Thermal guard rings with in-situ temperature sensors.

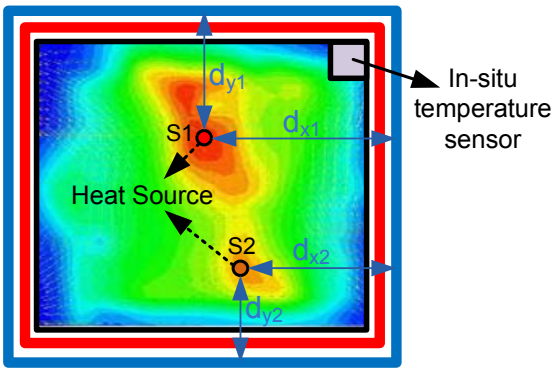

Fig. 5. Temperature detection with analytical model..

of the thermal guard ring. Therefore, each power-thermal domain can adjust its operation voltage and frequency based on the temperature information and workload.

The thermal guard ring is constructed by thermal vias connected from the substrate layer to the highest metal layer. The thermal guard ring is placed around the active circuits to transport heat to the thermal TSVs as shown in Fig. 4. For transferring signals between different power-thermal domains, the routing spaces should be reserved without thermal vias. Additionally, the highest metal layer is used to put a cover over a power-thermal domain as a thermal conductor to transport heat to thermal TSVs. Moreover, the thermal TSVs are inserted in the whitespace between two adjacent layers in 3D-ICs [6].

III. Analytical Model for Heat Dissipation in Power-Thermal Domain

Depending on the thermal guard ring, highest metal layer and thermal TSVs as shown in Fig. 2, an analytical model for on-chip heat dissipation in each power-thermal domain can be derived to calculate the offset temperatures between the hotspots and thermal guard ring. Since the highest metal and the guard ring are all composed of metal and attached together for each power-thermal domain as showed in Fig. 4, the five sides of the power-thermal domain can be assumed isothermal. While the bottom side is composed of silicon substrate, we assume the bottom side is adiabatic. Thus, most heat will transfer from the center to the guard ring and highest metal and dissipating to the outside environment through thermal TSVs.

We use the above assumptions as the boundary condition, defining the thermal distribution function with the position and the time variable as u(x,y,z,t), where {x, y, z} ∈ U, t > 0:

$$\cup = \left\{(x,y,z)\middle| -\frac{L}{2} \le x \le \frac{L}{2}, -\frac{L}{2} \le y \le \frac{L}{2}, -W \le z \le 0\right\} \quad (1)$$

In Eq. (1) where x, y, z means the coordinate of the die, t is the time and U means the global geometry of the die. L represents the length and width, and W represents the thickness of the die. Placing the temperature sensor near the guard ring in this structure as shown in Fig. 3, the temperature of the guard ring can be detected and feedback to the geometry. Based on this temperature information and the thermal distribution function of U at any given moment for t >0, the offset temperature between the hot spots and the guard ring can be easily calculated as shown in Fig. 5.

In order to get the approximate thermal distribution function u(x,y,z,t), the boundary condition of the partial differential equation should be considered. Since the boundary condition was prescribed by a Neumann problem (isothermal) on 5 sides, while a Dirichlet (adiabatic) problem on the bottom side, each side has been defined [13]. This analytical model has been validated in [13]. Now, the five sides of the power-thermal domain are assumed isothermal, and bottom side is assumed adiabatic. Moreover, from partial differential equation theory, this problem has a unique solution for U. Thus, we assume that

$$u(x,y,z,t) = u_1(x,t) \times u_2(y,t) \times u_3(z,t) \quad (2)$$

Then from Libniz rule, we know

$$\left(\Delta - \frac{\partial}{\partial t}\right) \cdot u(x,y,z,t)$$
$$= \left[\left(\Delta_x - \frac{\partial}{\partial t}\right) \cdot u_1(x,t)\right] \cdot u_2(y,t) \cdot u_3(z,t)$$
$$+ u_1(x,t) \cdot \left[\left(\Delta_y - \frac{\partial}{\partial t}\right) \cdot u_2(y,t)\right] \cdot u_3(z,t)$$
$$+ u_1(x,t) \cdot u_2(y,t) \cdot \left[\left(\Delta_z - \frac{\partial}{\partial t}\right) \cdot u_3(z,t)\right] \quad (3)$$

From the above equation, if we can find $u_1(x,t), u_2(y,t), u_3(z,t)$ which satisfy the previous boundary condition, we can solve the unique solution for u(x,y,z,t). Since $u_1(x,t), u_2(y,t), u_3(z,t)$ each has its own boundary condition on the geometry and time, we can use eigen function and eigen value method to solve $u_1(x,t), u_2(y,t), u_3(z,t)$ as below:

$$u_1(x,t) = 2 \cdot \sum_{k=0}^{\infty} e^{\frac{-4k^2\pi^2 t\gamma}{L^2}} \cos\left(\frac{2k\pi x}{L}\right) \quad (4)$$

$$u_2(y,t) = 2 \cdot \sum_{k=0}^{\infty} e^{\frac{-4k^2\pi^2 t\gamma}{L^2}} \cos\left(\frac{2k\pi y}{L}\right) \quad (5)$$

$$u_3(z,t) = 2 \cdot \sum_{k=0}^{\infty} e^{\frac{-4k^2\pi^2 t\gamma}{L^2}} \cos\left(\frac{(2k+1)\pi z}{2w}\right) \quad (6)$$

Combine these three equations, the thermal distribution function can be obtained as Eq. (7) for u(x,y,z,t).

$$u(x,y,z,t) = 8 \cdot \left[\sum_{k=0}^{\infty} e^{\frac{-4k^2\pi^2 t\gamma}{L^2}} \cos\left(\frac{2k\pi x}{L}\right)\right]$$
$$\times \left[\sum_{k=0}^{\infty} e^{\frac{-4k^2\pi^2 t\gamma}{L^2}} \cos\left(\frac{2k\pi y}{L}\right)\right]$$

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$$\times \left[\sum_{k=0}^{\infty} e^{\frac{-4k^2\pi^2 t_Y}{L^2}} \cos\left(\frac{(2k+1)\pi z}{2w}\right)\right] \quad (7)$$

Thus, with the thermal distribution function, we can easily calculate temperature offset between the hot spot and the guard. Accordingly, this information can be used to balance workloads in the overall system for further reducing temperature.

IV. Configuration of TSV 3D-ICs for Thermal Analysis

For demonstrating the proposed thermal control mechanism, an easy and accurate simulation method is adopted to model the full geometry of TSV 3D-ICs. Based on the same duality characteristics between the electrical circuit and heat dissipation model, the heat transfer plan can be easily modeled by the resistance and current source as shown in Fig. 6 [4]. In this simulation method, the fixed current source is modeled as the heat source which is generated at the hot spot. Thus, the electrical current through the resistance represents the heat flow through the material (thermal resistance). Accordingly, the voltage at each node can be the temperature at that node. Therefore, one way to simulate the temperature is to model the full geometry of TSV 3D-ICs as an electrical circuit composed of thermal resistances.

According to the TVS 3D-IC structure, the heat generated inside the working block is diffusive to the outside environment. In order to get the temperature of each point, the entire geometry is divided into small cubical thermal grids. Each grid is modeled by its equivalence electrical RC circuits with six resistances that represent the thermal dissipation path in six directions (top, bottom, east, south, west, north), and a capacitance that represents the heat storage at this grid as show in Fig.7(a). This node voltage can represent the temperature at this grid [14].

In the proposed TSV 3D-IC structure, all the thermal grids are classified into six cubes, including "heat sink, highest metal, thermal TSV, thermal guard ring, active circuit and substrate". And the thermal conductivities of the materials are listed in Table I. The materials of the "heat sink, highest metal and thermal guard ring" are copper, which has large thermal conductivity. According to the proposed TSV 3D-IC structure, combining these six cubes can form the thermal dissipation model with the thermal guard ring as show in Fig. 7(b). The active circuits in a power-thermal domain are encompassed by the thermal guard ring and the highest metal, and the material of the active circuits is the complex about the copper and S_iO_2.

V. Experimental Results

Depending on the configuration of TSV 3D-ICs described in Section IV, we constructed a TSV 3D-IC with 4 dies (4 layers) to demonstrate the proposed thermal control mechanism. The constructed TSV 3D-IC is based on back-to-face bonding technique as shown in Fig. 8. Fig. 8 also presents the thermal effect in a multi active region system, and each active region is a power-thermal domain. The gray part represents the active region in a power-thermal domain, including routing metals and active devices. The

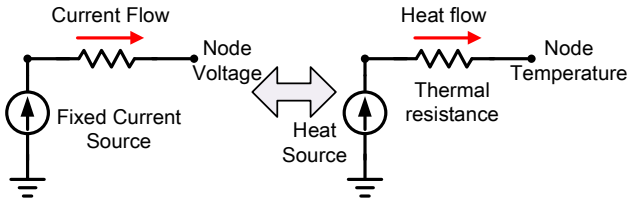

Fig. 6. Thermal guard rings with in-situ temperature sensors.

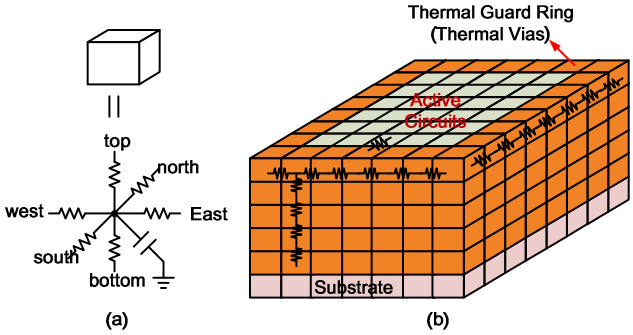

Fig. 7. (a) Equivalence electrical RC of a cube (b) Thermal dissipation model with the thermal guard ring

TABLE I
Thermal conductivities of the materials

Material	Thermal conductivity (W/mK)
Copper	398
S_iO_2	35
Substrate	15

orange squares present the thermal guard rings which are constructed by thermal vias. The blue part represents the whitespace to insert the thermal TSVs. In order to create thermal distribution model of the TSV 3D-IC, each power-thermal domain as a heater (hot spot) at a certain node to represent this point having a heavy workload. In each die, the circuits are divided into several power-thermal domains with different shapes to represent different functions. Moreover, the heat flows of heaters in the power-thermal domains are not the same. Consequently, the thermal guard rings (thermal via) are placed around thermal-power domains to offer thermal convection paths, while the whitespaces of the die are all placed by thermal TSVs.

For each die, we divide it into three major vertical levels: The top level is composed of the highest metal and thermal TSVs from the upper die; the middle level is constructed the thermal guard rings and active circuits; the bottom layer consists of the substrate and thermal TSVs. And the heat sink will connect to the top level of die-1 (layer-1).

According the above assumption structure and modeling, the temperature of each cubical cell can be easily measured. For demonstrating the thermal reduction of our proposed thermal control mechanism, we compared three different structures which are able to represent three real manufactured TSV 3D-ICs. The first TSV 3D-IC structure is developed without the thermal guard rings and thermal

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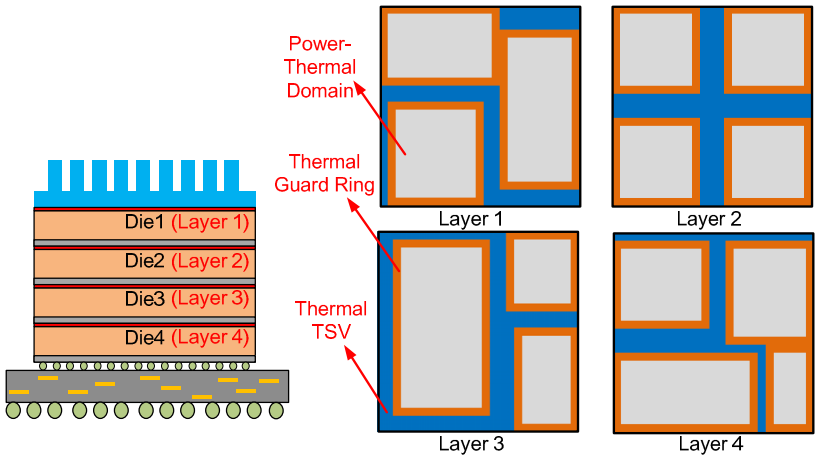

Fig. 8. Power-thermal domain setup in a 4-layer TSV 3D-IC with back-to-face bonding technique.

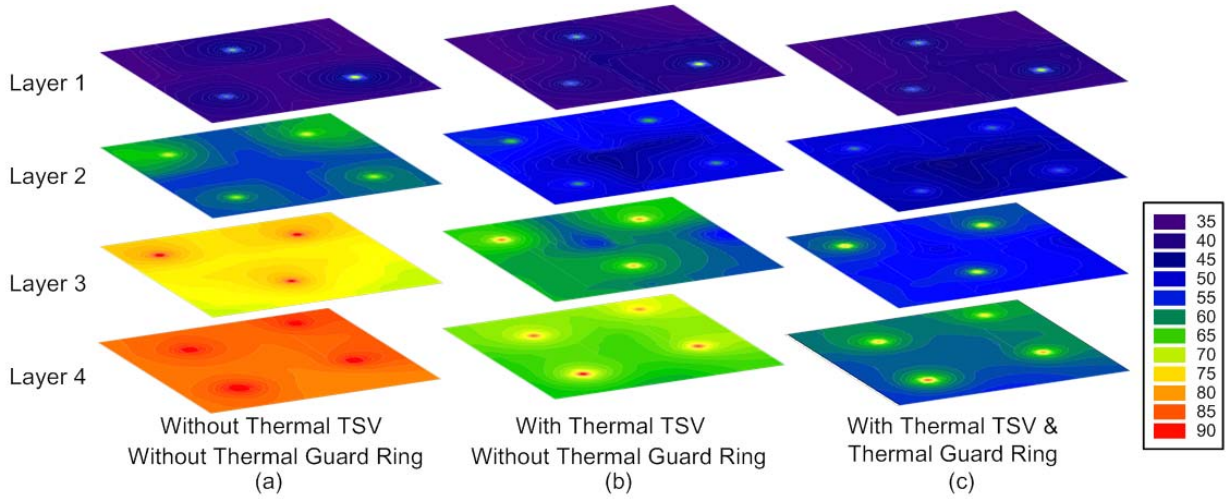

Fig. 9. Temperature distribution planes of three TSV 3D-IC structures (a) without the thermal guard rings and thermal TSVs (b) without thermal guard rings but with thermal TSVs (c) with both thermal guard rings and thermal TSVs.

TSVs both. And the second structure is developed without thermal guard rings but with thermal TSVs. The third TSV 3D-IC structure is the proposed one, which is constructed with both thermal guard rings and thermal TSVs.

Based on the configuration of TSV 3D-ICs and the setup of the power-thermal domains, Fig. 9 presents the temperature distribution planes of three TSV 3D-IC structures. From Fig. 9, heat will dissipate in all directions forming a concentric graph in the horizontal plane. However, in the vertical direction, since the thermal guard ring, thermal TSVs and the highest cover metal provide better convection paths, the average temperature are decreased for the upper dies. Table II lists the average temperature of each dies in the three TSV 3D-IC structures. Compared to the bottom layers, the temperatures of Die-1 to Die-3 are decreased by 43.96%, 16.56%, 9.4%, respectively.

TABLE II
The average temperature of each dies in the three TSV 3D-IC structures.

	Die-1	Die-2	Die-3	Die-4	Average temperature reduction in three structures
with both thermal guard ring & thermal TSV	38.10	47.39	54.13	58.40	-25.10%
Without thermal Guard ring but with thermal TSV	38.03	50.74	60.04	66.28	-17.38%
without both thermal guard ring & thermal TSV	38.07	57.96	74.04	83.65	0%
Temperature reduction compared to the bottom die	-43.96%	-24.34%	-9.40%	0%	

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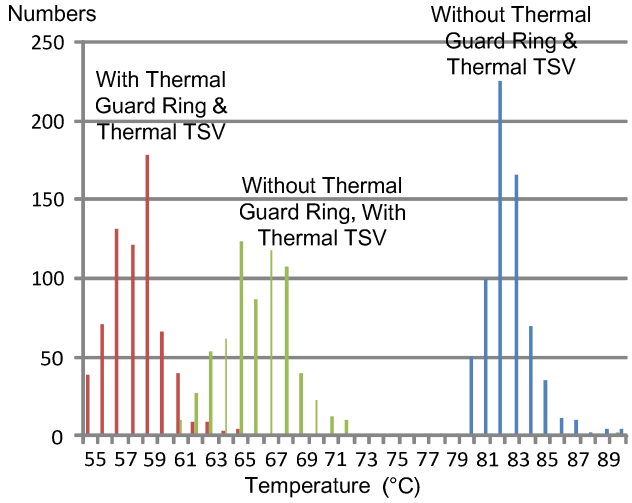

Fig. 10. Temperature scatter graph of layer-3 in the three TSV 3D-IC structures.

Table II also lists the comparisons of the three TSV 3D-IC structures. As we expected, since the thermal TSVs offer convection paths from lower dies to the heat sink, 17.38% temperature reduction can be achieved compared to the structure without the thermal guard rings and thermal TSVs. Furthermore, the thermal guard rings, highest cover metal and thermal TSVs form thermal convection paths from the active circuits (hotspots) to the heat sink. Hence, the proposed thermal control mechanism can further achieve about 25.10% temperature reduction compared to the structure without the thermal guard rings and thermal TSVs. Depending on the simulation results, we can effectively enhance thermal convection paths from the bottom die to the upper die through the thermal guard rings and thermal TSVs.

The temperature scatter graph of Layer-3 in the 3 TSV 3D-IC structures is as presented in Fig. 10. When the TSV 3D-IC structure is both without the thermal guard rings and thermal TSVs, the temperatures are scattered between 80°C ~90°C. The temperatures of the second structure which is only constructed by the thermal TSVs are scattered between 60°C~72°C. The temperatures of the third structure with both the thermal guard rings and thermal TSVs are distributed between 55°C~65°C. Moreover, the highest temperatures in each die have been removed to the lower temperature region using the proposed thermal control mechanism.

VI. CONCLUSIONS

For TSV 3D-ICs, stacking multiple dies faces a severe challenge of the thermal effect due to the low thermal conductivity of inter-layer dielectrics and high power density. In this paper, a thermal control mechanism with an in-situ temperature sensor for TSV 3D-ICs is presented using thermal guard rings and thermal TSVs. Depending on the thermal guard ring and thermal TSVs, an analytical model for on-chip heat dissipation in each power-thermal domain is also presented in this paper. Based on the analytical model, the offset temperatures between the hotspots in the power-thermal domain and thermal guard ring can be calculated. Therefore, the in-situ temperature sensor is placed near the thermal guard ring to detect the temperature and feedback the thermal information for the system. The simulation results show the thermal control mechanism with an in-situ temperature sensor can reduce temperature and detect heat dissipation of TSV 3D-ICs significantly. The proposed thermal control mechanism can further achieve about 25.10% temperature reduction. This technique can be extended to balance workloads in the overall system for further reducing temperature.

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